
**Identification cards — Optical memory
cards — Linear recording method —**

Part 4:

Logical data structures

*Cartes d'identification — Cartes à mémoire optique — Méthode
d'enregistrement linéaire —*

Partie 4: Structures de données logiques

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to the national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 11694-4 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Identification cards and related devices*.

ISO/IEC 11694 consists of the following parts, under the general title *Identification cards - Optical memory cards - Linear recording method*:

- Part 1: *Physical characteristics*
- Part 2: *Dimensions and location of the accessible optical area*
- Part 3: *Optical properties and characteristics*
- Part 4: *Logical data structures*

Annexes A and B form an integral part of this part of ISO/IEC 11694.

Introduction

This part of ISO/IEC 11694 is one of a series of standards describing the parameters for optical memory cards and the use of such cards for the storage and interchange of digital data.

The standards recognize the existence of different methods for recording and reading information on optical memory cards, the characteristics of which are specific to the recording method employed. In general, these different recording methods will not be compatible with each other. Therefore, the standards are structured to accommodate the inclusion of existing and future recording methods in a consistent manner.

This part of ISO/IEC 11694 is specific to optical memory cards using the linear recording method. Characteristics which apply to other specific recording methods shall be found in separate standards documents.

This part of ISO/IEC 11694 defines the logical data structures and the extent of compliance with, addition to, and/or deviation from the relevant base document ISO/IEC 11693.

The user's attention is called to the possibility that compliance with this part of ISO/IEC 11694 may require use of an invention covered by patent rights and/or other material covered by copyrights. By publication of this part of ISO/IEC 11694, no position is taken with respect to the validity of this claim or of any patent rights or copyrights in connection therewith.

Identification cards - Optical memory cards - Linear recording method -

Part 4: Logical data structures

1 Scope

This part of ISO/IEC 11694 defines the logical data structures for optical memory cards necessary to allow compatibility and interchange between systems using the linear recording method.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this part of ISO/IEC 11694. At the time of publication the editions indicated were valid. All standards are subject to revision and parties to agreements based on this part of ISO/IEC 11694 are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of ISO and IEC maintain registers of currently valid international standards.

ISO/IEC 11693:1994, *Identification cards - Optical memory cards - General characteristics*.

ISO/IEC 11694-1:1994, *Identification cards - Optical memory cards - Linear recording method - Part 1: Physical characteristics*.

ISO/IEC 11694-2:1995, *Identification cards - Optical memory cards - Linear recording method - Part 2: Dimensions and location of the accessible optical area*.

ISO/IEC 11694-3:1995, *Identification cards - Optical memory cards - Linear recording method - Part 3: Optical properties and characteristics*.

3 Definitions

For the purposes of this part of ISO/IEC 11694, the definitions given in ISO/IEC 11693, ISO/IEC 11694-1, ISO/IEC 11694-2, ISO/IEC 11694-3 and the following definitions apply.

3.1 data bit: An area which represents data on an optical memory card. A mark which has a different reflectivity and/or phase difference from the background reflectivity. One mark can define one or two data transitions dependent on the modulation method selected.

3.2 data track: The area located between adjacent track guides where data are written and/or read.

3.3 error correction code (ECC): A code designed to correct certain kinds of errors in data.

3.4 error detection and correction (EDAC): A family of methods in which redundancy is added to a message block, at the time the message block is recorded, in known fashion. Upon read back, a decoder removes the redundancy and uses the redundant information to detect and correct erroneous channel symbols.

3.5 modulation code: A system for coding which transforms information bits into some physical representation for recording onto the optical memory card.

3.6 pitch: The distance between corresponding points on adjacent data spots.

3.7 sector: The minimum unit of data that can be accessed on a card for any read and/or write command.

4 Reference points

The reference track and reference edges defined in ISO/IEC 11694-2 apply unless otherwise specified.

4.1 First data bit

The first data bit shall be located on the reference track and is part of the track ID. The location may vary dependent on the track layout selected. See annex A or annex B.

5 Track layout

Track layout information shall be preformatted on cards during manufacture and/or written to cards prior to use.

The total number of tracks may vary dependent on the application requirements; however, in all cases, tracks shall be arranged in order, and numbered sequentially, beginning with the reference track. See annex A or annex B for actual track layouts and numbering sequences.

5.1 Track layout options

See annex A or annex B for information concerning data structures that support the optional card layouts described in ISO/IEC 11694-2.

6 Track guides

Track guides shall be uniformly spaced across the card and shall extend the length of the accessible optical area. The accumulated tolerances across the width of all track guides shall be less than or equal to 24 μm at 25° C. See annex A or annex B for specific dimensions.

7 Guard tracks

There shall be 20 guard tracks, ten located directly above and ten directly below the user data area to enable the optics to locate the user data tracks and prevent the optical head from over running the accessible optical area if auto-tracking is lost.

Guard tracks may contain data relating to card type, physical data format, specific application and/or card drive autodiagnosis and calibration. See annex A or annex B.

8 Data tracks

Written and/or preformatted data shall be located within data tracks and centred between adjacent track guides to a tolerance of $\pm 0,5 \mu\text{m}$ in the y-axis. See annex A or annex B.

9 Track ID

Written and/or preformatted track ID shall identify the physical address of each data track. See annex A or annex B for specific configuration and location.

10 Sectors

Sectors are defined by the amount of user data in bytes and the number of sectors which can be written to a single data track. See annex A or annex B for specific types/sizes.

All sectors within a given track shall be identical in type and partially written tracks shall only be appended with sectors of the same type as those previously written on the track unless otherwise specified in annex A or annex B.

NOTE - Sector types/sizes have been defined to maximize the efficiency of data storage on a track and may vary by modulation code.

11 Data encoding

To encode data requires the use of a modulation code. See annex A or annex B for acceptable modulation codes.

NOTE - The user data on any single optical card shall only be encoded using one modulation code.

Annex A (normative)

8-10 NRZI modulation code, PWM recording method

A.1 Scope

This annex defines the logical data structures specific to optical cards using a pulse width modulation recording method and an 8-10 NRZI modulation code.

A.2 Definitions

For the purpose of this annex, the following definitions apply:

A.2.1 carrier/burst modulation code: A form of FM modulation code which makes 1,0 information correspond to a different frequency.

A.2.2 NRZI: Non-return-to-zero-inverse; a specific modulation method to make 1 corresponding to inverse and 0 to non-inverse.

A.2.3 Reed-Solomon code: A byte error detection and/or correction code which is generally used in optical and magnetic storage.

A.3 Reference points

The first bottom guard track (*LPT9*) is the reference track and shall be located $5,4 \text{ mm} \pm 0,3 \text{ mm}$ from the reference edge.

NOTE - This dimension is tighter yet still falls within the tolerance range specified by dimension *D* of ISO/IEC 11694-2.

A.3.1 First data bit

The first data bit closest the left edge of the card shall be located at $12,50 \text{ mm} \pm 0,40 \text{ mm}$ in the x-axis. The distance between the first data bit closest the left edge of the card and the first data bit closest the right edge of the card shall be $60,6 \text{ mm} \pm 0,1 \text{ mm}$ in the x-axis.

A.4 Track layout

Tracks shall be arranged in order beginning with the reference track and shall be numbered sequentially beginning with track -10, the reference track.

Track description	Track #	Hex
Guard track LPT9 (first bottom)	-10	FFF6
: :	:	:
Guard track LPT0 (last bottom)	-1	FFFF
First user data track	0	0000
: :	:	:
Last user data track	n	
Guard track UPT0 (first top)	n+1	
: :	:	:
Guard track UPT9 (last top)	n+10	

NOTE - Because the total number of tracks may vary dependent on the application requirements, the last user data track and the top guard tracks are expressed in parametric form.

A.5 Track layout options

This section provides information concerning data structures that support the optional card layouts described in ISO/IEC 11694-2.

A.5.1 Cards with moderate data capacity

This layout shall contain 2 520 data tracks, of which 2 500 shall be user data tracks. Tracks shall be numbered sequentially beginning with track -10, the reference track.

NOTE - This layout supports the inclusion of a magnetic stripe and/or signature panel.

A.5.2 Cards with options, no embossing

This layout shall contain 1 128 data tracks, of which 1 108 shall be user data tracks. Tracks shall be numbered sequentially beginning with track -10, the reference track.

NOTE - This layout supports the inclusion of a magnetic stripe, IC chip with contacts, and/or signature panel.

A.5.3 Cards with options, no IC chip

This layout shall contain 1 128 data tracks, of which 1 108 shall be user data tracks. Tracks shall be numbered sequentially beginning with track -10, the reference track.

NOTE - This layout supports the inclusion of a magnetic stripe, embossing, and/or signature panel.

The reference edges for this layout shall be the top edge and the right edge of the card. See ISO/IEC 11694-2.

For this layout, the first data bit closest the right edge of the card shall be located at $12,50 \text{ mm} \pm 0,40 \text{ mm}$ in the x-axis. The distance between the first data bit closest the right edge of the card and the first data bit closest the left edge of the card shall be $60,6 \text{ mm} \pm 0,1 \text{ mm}$ in the x-axis.

The track layout for these type cards shall be displayed from the top to the bottom of the card, beginning with the reference track.

A.5.4 Cards with maximum data capacity

This layout shall contain 3 593 data tracks, of which 3 573 shall be user data tracks. Tracks shall be numbered sequentially beginning with track -10, the reference track.

NOTE - This layout supports the inclusion of a magnetic stripe and/or signature panel.

A.6 Track guides

The width of the track guides shall be $2,3 \text{ } \mu\text{m} \pm 0,3 \text{ } \mu\text{m}$. The distance from the centre of one track guide to the centre of an adjacent track guide shall be $12,0 \text{ } \mu\text{m} \pm 0,2 \text{ } \mu\text{m}$.

No track guides shall have any breaks exceeding $180 \text{ } \mu\text{m}$.

A.7 Guard tracks

All guard tracks shall contain preformatted track-ID and card-type data and/or card-ID field data. Cards shall not be issued with these tracks left blank nor shall these tracks be made available to the application for writing.

Each guard track shall contain two track ID areas, one to the left, the other to the right of the card-type data and/or card-ID field. See A.10.

NOTE - It is expected that card drive units will have the ability to read guard tracks whether preformatted with card-type data or pre-recorded with card-ID field data.

A.7.1 Card-type data

Card-type data are pre-set indicia that denote the physical data format, the number and location of tracks and/or a specific type application. There shall be two blocks per track each containing the same card-type pattern repeated eight times. See figure A.1 and table A1.

Card-type data shall be preformatted using a carrier/burst modulation code. These tracks shall not be made available to the application for writing nor shall cards be issued with these tracks left blank.

The carrier/burst pattern shall consist of an *L*-pattern (denotes 0 data) and an *S*-pattern (denotes 1 data), the only difference between patterns being the pattern-pitch. The *L*-pattern pitch shall be $240 \text{ } \mu\text{m} \pm 5 \text{ } \mu\text{m}$ and the *S*-pattern pitch shall be $120 \text{ } \mu\text{m} \pm 5 \text{ } \mu\text{m}$. See A.12.2, figure A.1 and table A.1.

The length, or x-axis dimension, of preformatted data bits shall be $6,0 \text{ } \mu\text{m} \pm 0,6 \text{ } \mu\text{m}$; the width, or y-axis dimension, shall be $2,5 \text{ } \mu\text{m} \pm 0,5 \text{ } \mu\text{m}$; the bit pitch shall be $12,0 \text{ } \mu\text{m} \pm 0,3 \text{ } \mu\text{m}$. See figure A.1.

The distance between the first data bit of the left track ID closest the left edge of the card and the first data bit of the card type pattern closest the left edge of the card shall be $14,9 \text{ mm} \pm 0,1 \text{ mm}$ in the x-axis.

A.7.2 Unique card identification (ID) field

For those applications requiring unique card serialization, guard tracks *LPTI* (track -2) and *LPTO* (track -1) shall be used as a card-ID field. If using this option, information related to the application and other issuer information may be included in these tracks along with the card serialization data.

Card-ID field data shall be pre-recorded during the manufacturing process. These tracks shall not be made available to the application for writing nor shall cards be issued with these tracks left blank.

A.7.2.1 Content

Figure A.2 shows the structure and data content of the card-ID field. Data shall be pre-recorded using a type-2 sector as defined in A.11.1 and table A.2. The same information shall be repeated in each sector of each track, that is four times in two tracks.

NOTES

- 1 It is not permissible to set all data fields to *OFF* hex.
- 2 If no components of the card-ID field are used, these two tracks must be preformatted with card-type data. See A.7.1.

Field components include:

- **Application identifier (AID):** The AID shall consist of 16 bytes of alpha/numeric data, which data shall be agreed to by the card manufacturer and card issuer. If the AID is not implemented, these 16 bytes shall be set to *OFF* hex.

NOTE - Card manufacturers shall have the responsibility to manage the information to ensure AID's are not duplicated between different card issuers.

- **Unique identifier (UID):** The UID shall consist of six bytes, one byte containing the card manufacturer identifier (CMID), and five bytes containing a unique card identifier (UCID). If the UID is not implemented, these six bytes shall be set to *OFF* hex.

NOTES

- 1 The card manufacturer shall have the responsibility to ensure only one UID is contained in their card products.
- 2 Since different card manufacturers can use the same UCID, it is recommended that the entire UID (CMID + UCID) be used.

- **Number of issuer data bytes (NID):** The NID shall consist of two bytes which specify the number of bytes used in the ISSUER portion of the card-ID field. If the NID is not implemented, these two bytes shall be set to *OFF* hex.
- **Optional issuer data (ISSUER):** The ISSUER shall consist of 488 bytes and shall be reserved for the exclusive use of the card issuer. Any unused bytes in this area shall be set to *OFF* hex.

NOTE - Since card-ID field data are pre-recorded, the ISSUER data must be pre-recorded at the time of card manufacture.

A.8 Data tracks

Each data track can contain a maximum of 60,7 mm of written and/or preformatted data, including the gaps between sectors.

A.8.1 Data bits

Use of the 8-10 NRZI modulation code requires that written and/or preformatted data bits consist of four different sizes. The length, or x-axis dimension, shall be $3,0 \mu\text{m} \pm 0,6 \mu\text{m}$, $6,0 \mu\text{m} \pm 0,6 \mu\text{m}$, $9,0 \mu\text{m} \pm 0,6 \mu\text{m}$ or $12,0 \mu\text{m} \pm 0,6 \mu\text{m}$; the width, or y-axis dimension, shall be $2,5 \mu\text{m} \pm 0,5 \mu\text{m}$.

The minimum distance from the centre of one data bit to the centre of an adjacent data bit shall be $6,0 \mu\text{m} \pm 0,3 \mu\text{m}$.

A.9 Track components

A.9.1 Pre-amble (PRE)

A series of 60 consecutive bits laid out from the left edge direction of the card. The PRE bit-pattern shall be 101010101... or 0101010101... See figure A.3.

NOTE - The PRE generates the data clock required by the card drive's phase-lock-loop (PLL) circuit when an optical card is read from left to right.

A.9.2 Sync marker

A specific 10-bit pattern which does not show up as a read-output signal when the 8-10 NRZI modulation code is implemented on the track ID and/or user data.

NOTE - When asynchronization occurs during reading, data can be re-synchronized after sensing successive sync markers.

The sync marker shall be set on the border of the data matrix, created when implementing the Reed-Solomon code, to divide the user data into multiple blocks. See figure A.4.

The first sync marker from the left edge of the card, in every sector and in both track ID's, shall be 1100010001 prior to NRZI modulation. All other sync markers shall be either 1100010001 or 0100010001 prior to NRZI modulation.

Thus all written sync markers shall become either 1000011110 or 0111100001 after NRZI modulation.

A.9.3 Post-amble (PST)

A series of 60 consecutive bits laid out from the left edge direction of the card. The PST bit-pattern shall be 0101010101... or 1010101010... See figure A.3.

NOTE - The PST generates the data clock required by the card drive's PLL circuit when an optical card is read from right to left.

A.10 Track ID

Track ID shall be preformatted at the right and left side of each data track. See figures A.3 and A.5.

NOTE - The structure allows the track ID to be read from either direction, that is from left to right or right to left.

A.10.1 Content

The track ID shall consist of 75 bytes of information and the length shall be $2,25 \text{ mm} \pm 0,02 \text{ mm}$. The track ID shall consist of the PRE, sync markers, track numbers, ECC and the PST. See A.12.3 and figure A.3.

The track number itself shall be repeated twice per track ID with the most significant bit (MSB) positioned closest the left edge of the card.

A.11 Sectors

Every sector shall contain a PRE, sync markers, user data, ECC and a PST and shall be separated from adjoining sectors

by a gap, that is an unrecorded area. See figures A.4 and A.5.

User data shall be written within a sector and arranged from left to right regardless of the writing direction implemented.

NOTE - Sectors can be written in either direction, that is, from left to right, the forward direction, or from right to left, the reverse direction.

The accumulated tolerances across any sector shall be less than $\pm 3\%$ of the sector length.

A.11.1 Types of sectors

Sector types shall be as defined in figure A.6 and table A.2.

NOTE - The sector lengths shown in figure A.6 are the maximum allowed when taking into consideration up to a 3 % deviation in the velocity of the card drive mechanism which is anticipated in the actual use of optical card systems.

All sectors, regardless of sector type, shall be located relative to the first bit position of the left track ID. The MSB shall always be placed at the edge of each sector closest the left edge of the card.

A.12 Data encoding

This section describes the method for encoding and storing data on optical cards using the various sector types.

A.12.1 Modulated data

All track ID's and user data along with their associated ECC shall be modulated using the 8-10 NRZI modulation code. See figures A.7, A.8, A.9 and table A.3.

NOTE - When encoding, ten bits are assigned to every eight bits of actual data using the 8-10 modulation table. When reading, the original eight bits are retrieved/demodulated from the corresponding 10-bit data pattern.

A.12.2 Carrier/burst modulation code

All card-type data shall be preformatted using the carrier/burst modulation code. See A.7.1, figure A.1 and table A.1.

NOTE - In the read mode, this modulation code permits card-type information found in the guard tracks to be demodulated with software, eliminating the influence from the variable velocity, if any, of the optical card drive.

A.12.3 Error correction code

Each track ID and every sector of written data shall be encoded using the Reed-Solomon ECC generated by the following generator polynomial:

$$G(x) = (X - \alpha^3) (X - \alpha^2) (X - \alpha) (X - 1)$$

where

$$x^8 + x^4 + x^3 + x^2 + 1 = 0$$

α is a primitive element of $GF(2^8)$.

The Reed-Solomon code arranges every track ID and every sector of user data into a matrix as shown in figure A.10 and then applies the ECC based on the generator polynomial, resulting in the addition of four parity bytes to the matrix.

EXAMPLE - Track ID are encoded using a C1 (6,2), C2 (6,1) Reed-Solomon code. As a result, 28 parity bytes are added to the original two bytes which make up the track ID.

EXAMPLE - Encoding a sector type 7 using the Reed-Solomon ECC.

Write 16 bytes of data containing the following integer values in hexadecimal:

00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F

Arranging the bytes into an 8 x 2 matrix, the data becomes:

00	01	02	03	04	05	06	07
08	09	0A	0B	0C	0D	0E	0F

Encoding each row of the matrix using the generator polynomial $G(x)$, the above matrix becomes:

00	01	02	03	04	05	06	07	2C	84	05	AD
08	09	0A	0B	0C	0D	0E	0F	D8	4E	65	F3

Encoding each column of this matrix using the generator polynomial $G(x)$, the matrix becomes:

00	01	02	03	04	05	06	07	2C	84	05	AD
08	09	0A	0B	0C	0D	0E	0F	D8	4E	65	F3
78	14	A0	CC	D5	B9	0D	61	EE	FB	DB	CE
AD	CC	6F	0E	34	55	F6	97	18	91	77	FE
E7	4D	AE	04	75	DF	3C	96	67	8F	E8	00
3A	9D	69	CE	9C	3B	CF	68	65	2F	24	6E

A.13 Measurement

NOTES

- 1 The reading/writing test conditions outlined in ISO/IEC 11694-3 apply unless otherwise specified when observing the optical characteristics.
- 2 An Optical Specialties, Inc. Video Linewidth System, VLS-I, or equivalent, is used for physical measurements.

A.13.1 Track guide measurement

The measurement of the track guide pitch and width shall be performed in the nine areas shown in figure A.11. Each area shall consist of ten tracks and the average value at each of the nine areas shall fall within the specified range.

A.13.2 Track ID measurement

The measurement of the track ID data bit size, bit pitch and the length of the track ID shall be performed in the six areas

designated by *D* and *E* in figure A.11. Each area shall consist of ten tracks and the average value at each of the six areas shall fall within the specified range.

A.13.3 Guard track measurement

The measurement of the guard track data bit size, bit pitch and the carrier pattern pitch shall be performed in two tracks each in the areas designated *A* and *C* in figure A.11. The average value of a minimum of ten measurements taken at each location shall fall within the specified range.

A.13.4 Preformatted data characteristics

The following characteristics shall be achieved when scanning a preformatted portion of the accessible optical area containing a card-type carrier/burst pattern. See figure A.1.

To achieve the expected results, tests shall be conducted using a beam diameter of $2,5\ \mu\text{m}$ and a media linear velocity of $480\ \text{mm/s} \pm 3\%$.

A.13.4.1 The low frequency recovery value shall be greater than or equal to 0,9. See ISO/IEC 11694-3.

A.13.4.2 The amplitude comparison value shall be greater than or equal to 0,8. See ISO/IEC 11694-3.

A.13.4.3 The signal overlap (S_o) divided by the high frequency amplitude (A_{HF}) shall be greater than or equal to 0,8. See ISO/IEC 11694-3.

A.13.5 Written data measurement

The measurement of the written data bit and the bit pitch shall

be determined using the wave shape of the read out signal using a beam diameter of $2,5\ \mu\text{m}$, a read power of $0,1\ \text{mW} \pm 5\%$ and a media linear velocity of $480\ \text{mm/s} \pm 0,5\%$.

The bit size shall be measured at the half value point and the bit pitch at the peak point of the read signal. The average value of a minimum of ten measurements shall fall within the specified range.

A.13.6 Written data characteristics

The following characteristics shall be achieved when scanning a written portion of the accessible optical area containing high frequency data (80 kHz), and low frequency data (20 kHz).

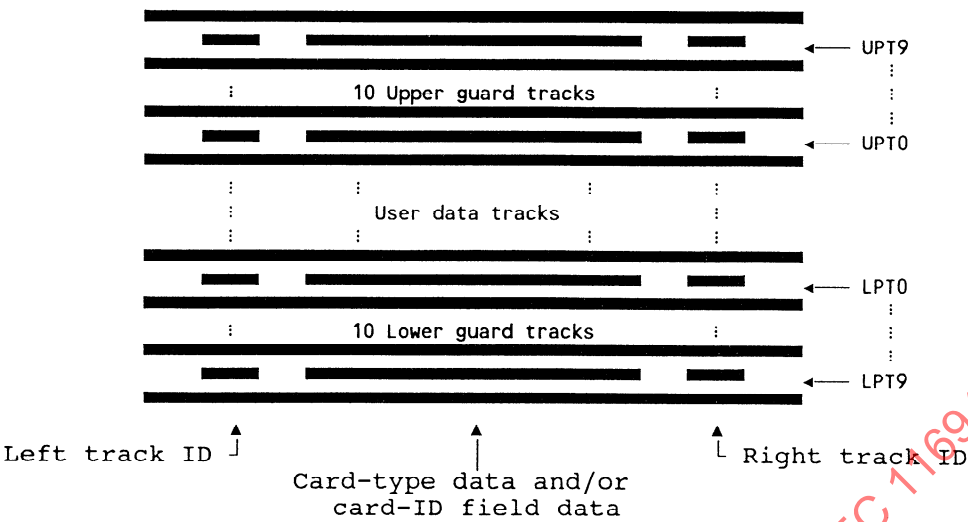
To achieve the expected results, tests shall be conducted using a beam diameter of $2,5\ \mu\text{m}$ and a media linear velocity of $480\ \text{mm/s} \pm 3\%$. The write power shall be $18\ \text{mW} \pm 5\%$. A pulse width of $3,5\ \mu\text{s}$ at 80 kHz, and $22\ \mu\text{s}$ at 20 kHz shall be used.

A.13.6.1 The low frequency recovery value shall be greater than or equal to 0,9. See ISO/IEC 11694-3.

A.13.6.2 The amplitude comparison value shall be greater than or equal to 0,8. See ISO/IEC 11694-3.

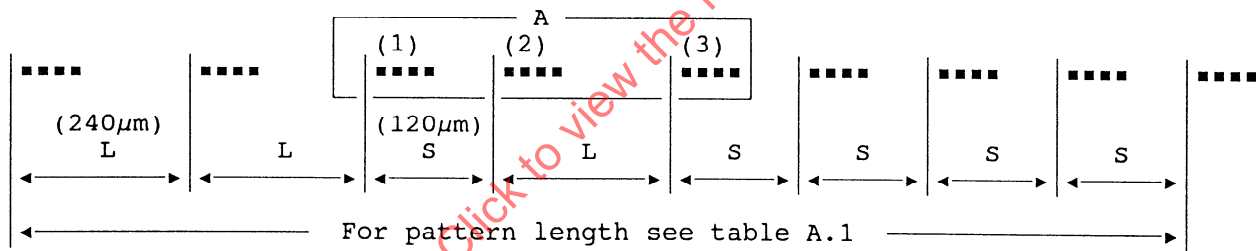
A.13.6.3 The signal overlap (S_o) divided by the high frequency amplitude (A_{HF}) shall be greater than or equal to 0,8. See ISO/IEC 11694-3.

A.13.6.4 The carrier-to-noise ratio (C/N) shall be greater than or equal to 40 dB when measured across a bandwidth 1 kHz at a carrier frequency of 80 kHz.



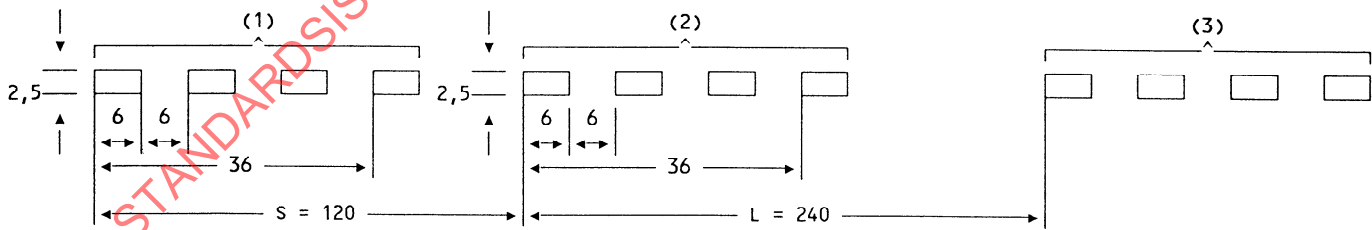
NOTE - LPT9 is the reference track as described in ISO/IEC 11694-2.

(a) Guard track layout



Detail A

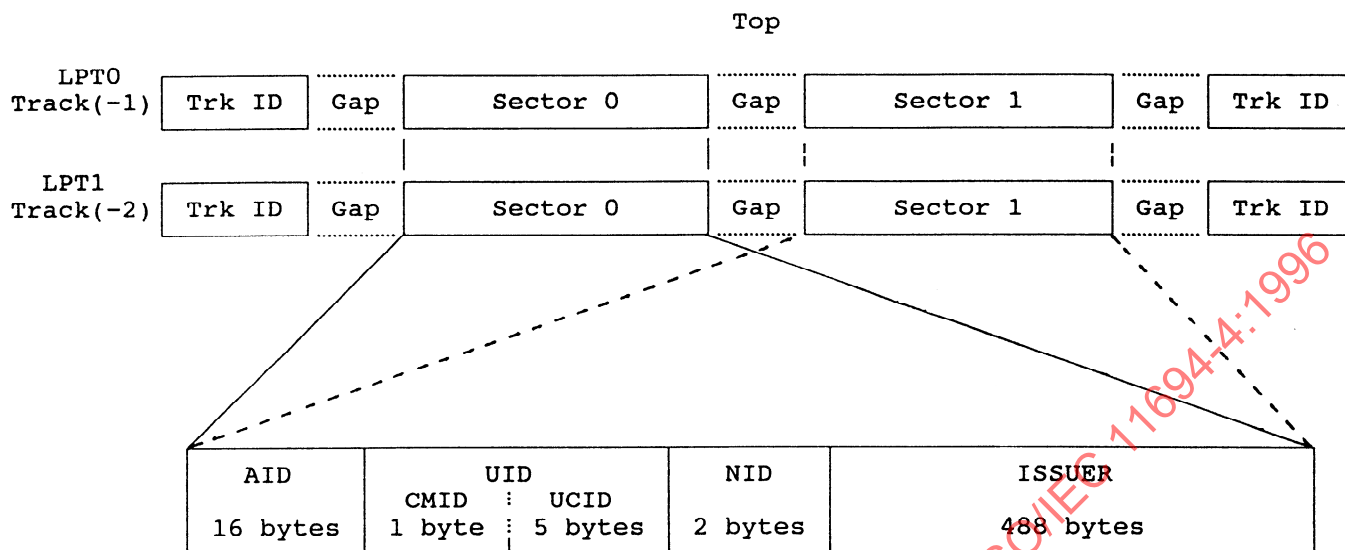
Dimensions in micrometres.



(b) Example of card-type pattern (P11) - See table A.1

NOTE - Drawings not to scale.

Figure A.1 - Guard track structure



NOTE - Type-2 sectors shall be used for card-ID field data.

(a) Structure of each sector in the card-ID field

Length	Field name	Description	Control
16	AID	Application identifier	Mfg/Isr
1	CMID	Card manufacturer identifier	Std
5	UCID	Unique card identifier	Mfg
2	NID	Number of issuer data bytes	Isr
488	ISSUER	Reserved for issuer data	Isr

NOTES

- 1 *Length* values are in bytes.
- 2 *Mfg* are fields assigned/controlled by each individual card manufacturer.
- 3 *Isr* are fields assigned/controlled by each individual card issuer.
- 4 *Std* are fields assigned/controlled by the appropriate ISO/IEC standards body.

(b) Content of the card-ID field

Figure A.2 - Structure and content of the card-ID field

Left edge

PRE 1010101010...or 0101010101... 60 bits	S y n c	Track number 20 bits	E C C 280 bits	S y n c	Track number 20 bits	E C C 280 bits	S y n c	PST 1010101010...or 0101010101... 60 bits	Gap
--	------------------	----------------------------	-------------------	------------------	----------------------------	-------------------	------------------	--	-----

Gap	PRE 1010101010...or 0101010101... 60 bits	S y n c	Track number 20 bits	E C C 280 bits	S y n c	Track number 20 bits	E C C 280 bits	S y n c	PST 1010101010...or 0101010101... 60 bits
-----	--	------------------	----------------------------	-------------------	------------------	----------------------------	-------------------	------------------	--

Right edge

NOTE - Each sync pattern is 10 bits set to 1000011110 or 0111100001.

Figure A.3 - Track ID format

Left edge

PRE	Sync	Block 1	Sync	Block 2	Sync	Block 3	Sync		Sync	Block <i>m</i>	Sync	PST
-----	------	---------	------	---------	------	---------	------	--	------	----------------	------	-----

NOTE - *m* denotes *m* in table A.2.

Figure A.4 - Format of a sector

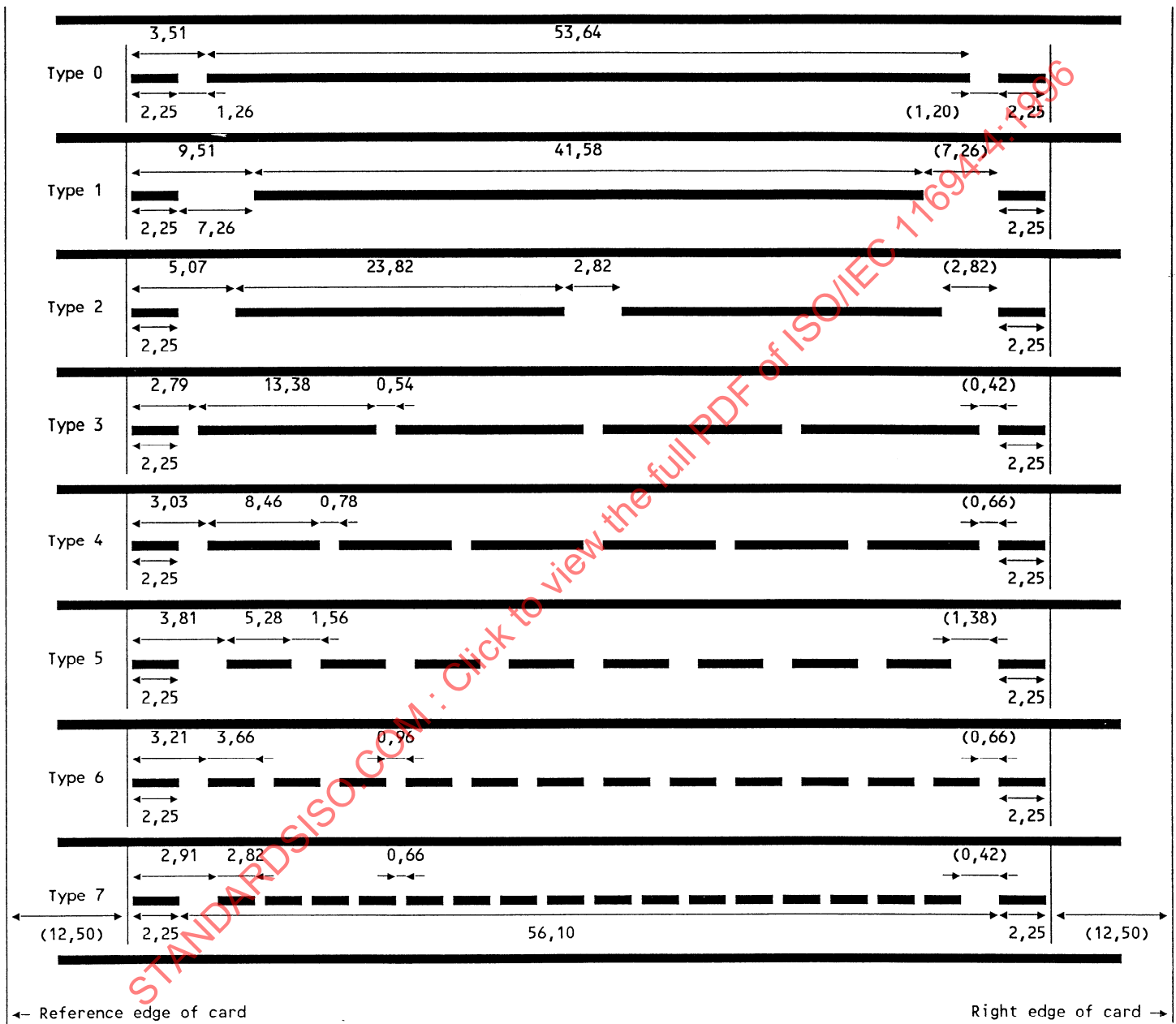
Left edge

Track ID	Gap	Sector 1	Gap	Sector 2	Gap		Gap	Sector <i>n</i>	Gap	Track ID
----------	-----	----------	-----	----------	-----	--	-----	-----------------	-----	----------

NOTE - *n* denotes *n* in table A.2.

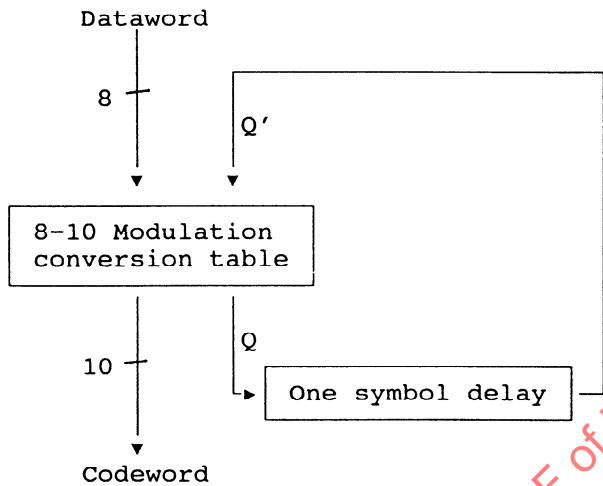
Figure A.5 - Format of a data track

Dimensions in millimetres.



NOTE - Drawing not to scale.

Figure A.6 - Sector layout by type



EXAMPLE

Dataword		Sync ($Q' = -1$)	FF ($Q' = 1$)	FF ($Q' = -1$)									
Q output	-1	1	-1	-1									
Codeword		0 1 0 0 0 1 0 0 0 1	0 1 1 1 1 0 1 0 1 0	1 1 1 1 1 0 1 0 1 0									
Modulated waveform													

NOTES

- 1 The 8-10 modulation conversion table is shown in table A.3.
- 2 The codeword is selected by the dataword and Q' . Q' is the Q output of the previous codeword.
- 3 The modulated waveform is made from the codeword stream according to the NRZI rule.

Figure A.7 - 8-10 modulation method

ECC encoding:

```

04 E2 46 A0 99 99
3C D7 C5 2E 54 54
D8 E1 B5 8C DE DE
FD F6 66 6D 9A 9A
1D 22 50 6F 89 89

```

8-10 modulation plus sync markers:

```

0101001001 1111011101 xxxxxecc00 xxxxxecc01 xxxxxecc02 xxxxxecc03
xxxxxecc04 xxxxxecc05 xxxxxecc06 xxxxxecc07 xxxxxecc08 xxxxxecc09
xxxxxecc10 xxxxxecc11 xxxxxecc12 xxxxxecc13 xxxxxecc14 xxxxxecc15
xxxxxecc16 xxxxxecc17 xxxxxecc18 xxxxxecc19 xxxxxecc20 xxxxxecc21
xxxxxecc22 xxxxxecc23 xxxxxecc24 xxxxxecc25 xxxxxecc26 xxxxxecc27
xxxxsyncx 0101001001 1111011101 xxxxxecc00 xxxxxecc01 xxxxxecc02
xxxxxecc03 xxxxxecc04 xxxxxecc05 xxxxxecc06 xxxxxecc07 xxxxxecc08
xxxxxecc09 xxxxxecc10 xxxxxecc11 xxxxxecc12 xxxxxecc13 xxxxxecc14
xxxxxecc15 xxxxxecc16 xxxxxecc17 xxxxxecc18 xxxxxecc19 xxxxxecc20
xxxxxecc21 xxxxxecc22 xxxxxecc23 xxxxxecc24 xxxxxecc25 xxxxxecc26
xxxxxecc27 xxxxxsyncx

```

NRZI conversion plus PRE, sync and PST patterns:

```

1010101010 1010101010 1010101010 1010101010 1010101010 1010101010
xxxxsyncx xxxtr#high xxxtr#low xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxsyncx xxxtr#high xxxtr#low xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi xxxxxnrzi
xxxxxxnrzi xxxxxnrzi xxxxxsyncx 0101010101 0101010101 0101010101
0101010101 0101010101 0101010101

```

Figure A.8 - Example of modulation code using the track ID # 1250 (04E2 hex)

ECC encoding:

D00	D01	D02	D03	D04	D05	D06	D07	E00	E01	E02	E03
D08	D09	D10	D11	D12	D13	D14	D15	E04	E05	E06	E07
D16	D17	D18	D19	D20	D21	D22	D23	E08	E09	E10	E11
D24	D25	D26	D27	D28	D29	D30	D31	E12	E13	E14	E15
D32	D33	D34	D35	D36	D37	D38	D39	E16	E17	E18	E19
D40	D41	D42	D43	D44	D45	D46	D47	E20	E21	E22	E23
D48	D49	D50	D51	D52	D53	D54	D55	E24	E25	E26	E27
D56	D57	D58	D59	D60	D61	D62	D63	E28	E29	E30	E31
E32	E33	E34	E35	E36	E37	E38	E39	E40	E41	E42	E43
E44	E45	E46	E47	E48	E49	E50	E51	E52	E53	E54	E55
E56	E57	E58	E59	E60	E61	E62	E63	E64	E65	E66	E67
E68	E69	E70	E71	E72	E73	E74	E75	E76	E77	E78	E79

8-10 modulation plus sync markers:

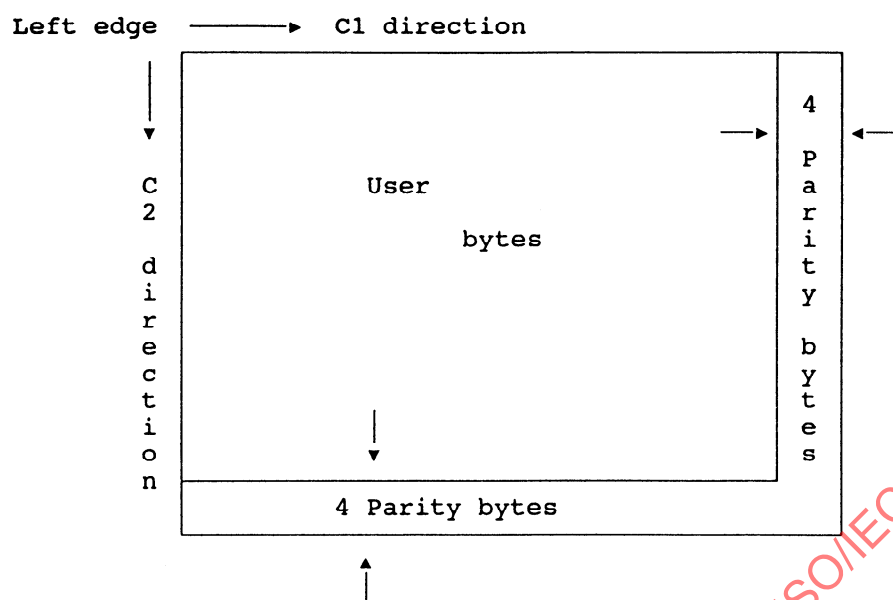
MD00	MD01	MD02	MD03	MD04	MD05	MD06	MD07	ME00	ME01	ME02	ME03	SYNC
MD08	MD09	MD10	MD11	MD12	MD13	MD14	MD15	ME04	ME05	ME06	ME07	SYNC
MD16	MD17	MD18	MD19	MD20	MD21	MD22	MD23	ME08	ME09	ME10	ME11	SYNC
MD24	MD25	MD26	MD27	MD28	MD29	MD30	MD31	ME12	ME13	ME14	ME15	SYNC
MD32	MD33	MD34	MD35	MD36	MD37	MD38	MD39	ME16	ME17	ME18	ME19	SYNC
MD40	MD41	MD42	MD43	MD44	MD45	MD46	MD47	ME20	ME21	ME22	ME23	SYNC
MD48	MD49	MD50	MD51	MD52	MD53	MD54	MD55	ME24	ME25	ME26	ME27	SYNC
MD56	MD57	MD58	MD59	MD60	MD61	MD62	MD63	ME28	ME29	ME30	ME31	SYNC
ME32	ME33	ME34	ME35	ME36	ME37	ME38	ME39	ME40	ME41	ME42	ME43	SYNC
ME44	ME45	ME46	ME47	ME48	ME49	ME50	ME51	ME52	ME53	ME54	ME55	SYNC
ME56	ME57	ME58	ME59	ME60	ME61	ME62	ME63	ME64	ME65	ME66	ME67	SYNC
ME68	ME69	ME70	ME71	ME72	ME73	ME74	ME75	ME76	ME77	ME78	ME79	SYNC

NRZI conversion plus PRE, sync, PST patterns:

PRE1	PRE2	PRE3	PRE4	PRE5	PRE6	SYNC	MD00	MD01	MD02	MD03	MD04	MD05
MD06	MD07	ME00	ME01	ME02	ME03	SYNC	MD08	MD09	MD10	MD11	MD12	MD13
MD14	MD15	ME04	ME05	ME06	ME07	SYNC	MD16	MD17	MD18	MD19	MD20	MD21
MD22	MD23	ME08	ME09	ME10	ME11	SYNC	MD24	MD25	MD26	MD27	MD28	MD29
MD30	MD31	ME12	ME13	ME14	ME15	SYNC	MD32	MD33	MD34	MD35	MD36	MD37
MD38	MD39	ME16	ME17	ME18	ME19	SYNC	MD40	MD41	MD42	MD43	MD44	MD45
MD46	MD47	ME20	ME21	ME22	ME23	SYNC	MD48	MD49	MD50	MD51	MD52	MD53
MD54	MD55	ME24	ME25	ME26	ME27	SYNC	MD56	MD57	MD58	MD59	MD60	MD61
MD62	MD63	ME28	ME29	ME30	ME31	SYNC	ME32	ME33	ME34	ME35	ME36	ME37
ME38	ME39	ME40	ME41	ME42	ME43	SYNC	ME44	ME45	ME46	ME47	ME48	ME49
ME50	ME51	ME52	ME53	ME54	ME55	SYNC	ME56	ME57	ME58	ME59	ME60	ME61
ME62	ME63	ME64	ME65	ME66	ME67	SYNC	ME68	ME69	ME70	ME71	ME72	ME73
ME74	ME75	ME76	ME77	ME78	ME79	SYNC	PRE1	PRE2	PRE3	PRE4	PRE5	PRE6

* MDxx, MExx : 10 bits

Figure A.9 - Example of modulation code using a sector type 5



(a) Sector layout with ECC applied

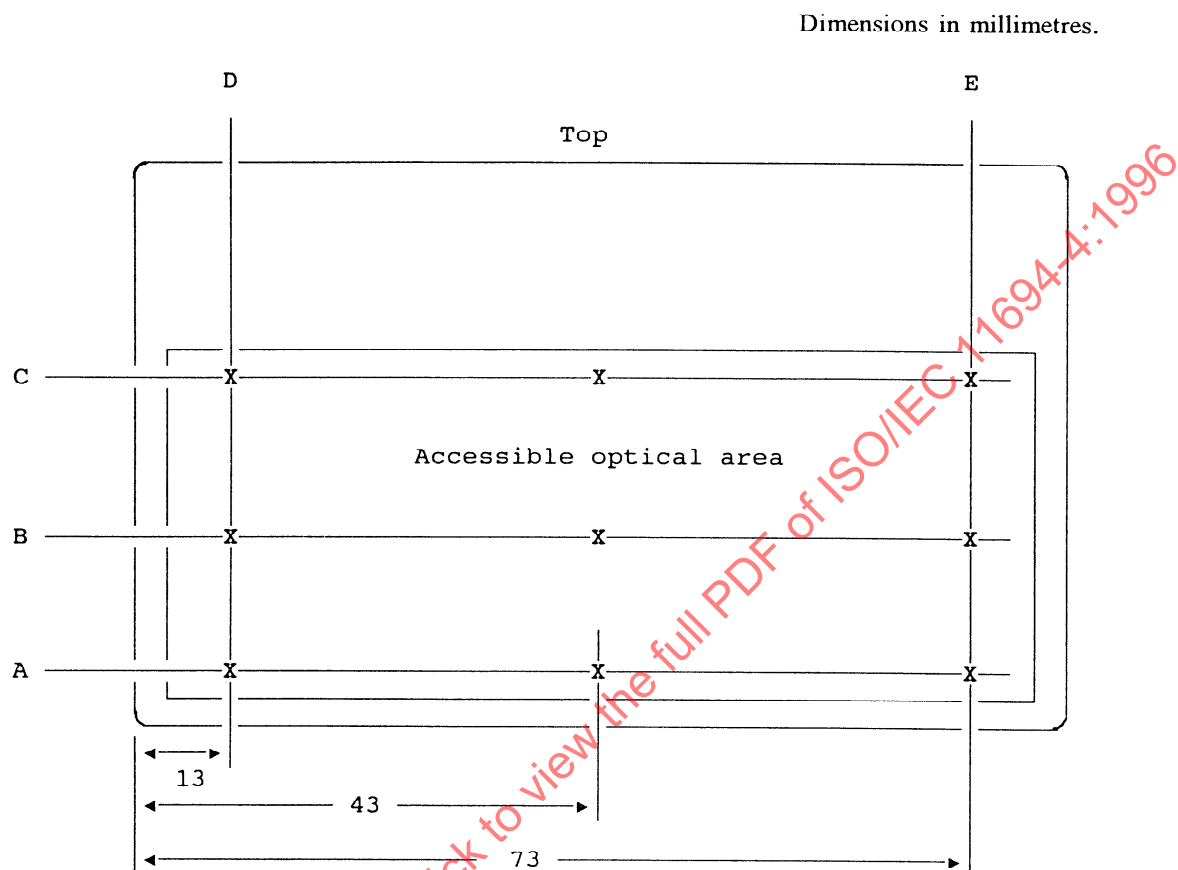
Type	User bytes per sector	Parity bytes per sector	Structure of ECC in bytes	
			(direction)	(direction)
Sector type 0	1368	312	C1(40,36)	C2(42,38)
Sector type 1	1024	272	C1(36,32)	C2(36,32)
Sector type 2	512	208	C1(20,16)	C2(36,32)
Sector type 3	256	144	C1(20,16)	C2(20,16)
Sector type 4	128	112	C1(12,8)	C2(20,16)
Sector type 5	64	80	C1(12,8)	C2(12,8)
Sector type 6	32	64	C1(12,8)	C2(8,4)
Sector type 7	16	56	C1(12,8)	C2(6,2)

(b) Content of sector with ECC applied

Type	Bytes per ID	Parity bytes per ID	Structure of ECC	
			(direction)	(direction)
Track ID	2	28	C1(6,2)	C2(5,1)

(c) Content of track ID with ECC applied

Figure A.10 - ECC matrix



NOTES

- 1 Drawing not to scale.
- 2 *A* designates the lower guard track area.
- 3 *B* designates the center region of the user data track area.
- 4 *C* designates the upper guard track area.
- 5 *B* and *C* shall vary according to card type.
- 6 *D* designates the left track ID area.
- 7 *E* designates the right track ID area.

Figure A.11 - Measurement points

Table A.1 (a) - Guard tracks - Structure of card-type data

First block			Second block		
H	P x 8	H	H	P x 8	T

NOTE - *P* is the card-type pattern and shall vary by card type.

Table A.1 (b) - Guard tracks - Configuration of card-type pattern

Card type	Card-type pattern (P) See figure A.1	Pattern length (in μm)	Length of 1st block (in μm)	Length of 2nd block (in μm)	TNmax	Total tracks	GYupper (in mm) ($\pm 0,3\text{mm}$)
0	LLLLLLSS	1680	15360	15480	R E S E R V E D		
1	LLLLLSSS	1560	14400	14520	2509	2520	35,6
2	LLLLSLSS	1560	14400	14520	3582	3593	48,5
3	LLLLSSSS	1440	13440	13560	1117	1128	18,9
4	LLLSLLSS	1560	14400	14520	**	**	**
5	LLLSLSSS	1440	13440	13560	**	**	**
6	LLLSSLSS	1440	13440	13560	**	**	**
7	LLSSSSSS	1320	12480	12600	**	**	**
8	LLSLLLSS	1560	14400	14520	**	**	**
9	LLSLLSSS	1440	13440	13560	**	**	**
10	LLSLSLSS	1440	13440	13560	**	**	**
11	LLSLSSSS	1320	12480	12600	**	**	**
12	LLSSLSSS	1440	13440	13560	**	**	**
13	LLSSLSSS	1320	12480	12600	**	**	**
14	LLSSSLSS	1320	12480	12600	**	**	**
15	LLSSSSSS	1200	11520	11640	**	**	**
H	SSSSSSSS	960	-	-	-	-	-
T	SSSSSSSS	1080	-	-	-	-	-

NOTES

- 1 *S* denotes a short pattern pitch (120 μm); *L* denotes a long pattern pitch (240 μm).
- 2 *TNmax* is the maximum value assigned a track number, the last upper guard track (UPT9), using a specific card type pattern.
- 3 *GYupper* is the location, the y-axis measurement from the reference edge, of the last upper guard track (UPT9).
- 4 ** These fields are determined by the application and shall be assigned and controlled by the card manufacturer in conjunction with the card issuer.

Table A.2 - Structure of the sectors

Sector type	User bytes per sector	Bytes per block	Blocks per sector (m)	Sectors per track (n)	Bytes per sector with ECC	Total bytes per sector
Type 0	1368	40	42	1	1680	1735
Type 1	1024	36	36	1	1296	1345
Type 2	512	20	36	2	720	769
Type 3	256	20	20	4	400	433
Type 4	128	12	20	6	240	273
Type 5	64	12	12	8	144	169
Type 6	32	12	8	12	96	117
Type 7	16	12	6	16	72	91
NOTES 1 <i>User bytes per sector</i> is the number of user bytes available after ECC has been applied. 2 <i>m</i> denotes the number of data blocks per sector. See figure A.4. 3 <i>n</i> denotes the number of sectors allowed per track. See figure A.5. 4 <i>Total bytes per sector</i> includes PRE, PST and sync markers.						

Table A.3 - 8-10 modulation conversion table

Q' = -1				Q' = 1				Q' = -1				Q' = 1			
Dataword	Codeword	DC	Q	Codeword	DC	Q		Dataword	Codeword	DC	Q	Codeword	DC	Q	
MSB-LSB	MSB - LSB			MSB - LSB				MSB-LSB	MSB - LSB			MSB - LSB			
00	00000000	0101010101	0	1	0101010101	0	-1	28	00101000	0111110101	0	1	0111110101	0	-1
01	00000001	0101010111	0	-1	0101010111	0	1	29	00101001	0111110111	0	-1	0111110111	0	1
02	00000010	0101011101	0	-1	0101011101	0	1	2A	00101010	0111111101	0	-1	0111111101	0	1
03	00000011	0101011111	0	1	0101011111	0	-1	2B	00101011	0111111111	0	1	0111111111	0	-1
04	00000100	0101001001	0	-1	0101001001	0	1	2C	00101100	0111101001	0	-1	0111101001	0	1
05	00000101	0101001011	0	1	0101001011	0	-1	2D	00101101	0111101011	0	1	0111101011	0	-1
06	00000110	0101001110	0	1	0101001110	0	-1	2E	00101110	0111101110	0	1	0111101110	0	-1
07	00000111	0101011010	0	1	0101011010	0	-1	2F	00101111	0111111010	0	1	0111111010	0	-1
08	00001000	0101110101	0	-1	0101110101	0	1	30	00110000	0111010010	0	1	0111010010	0	-1
09	00001001	0101110111	0	1	0101110111	0	-1	31	00110001	0111010011	2	-1	0111010011	-2	-1
0A	00001010	0101111101	0	1	0101111101	0	-1	32	00110010	0111010010	0	-1	0111010010	0	1
0B	00001011	0101111111	0	-1	0101111111	0	1	33	00110011	0111010011	0	1	0111010011	0	-1
0C	00001100	0101101001	0	1	0101101001	0	-1	34	00110100	0111110001	2	1	0111110001	-2	1
0D	00001101	0101101011	0	-1	0101101011	0	1	35	00110101	0111110011	2	-1	0111110011	-2	-1
0E	00001110	0101101110	0	-1	0101101110	0	1	36	00110110	0111110110	2	-1	0111110110	-2	-1
0F	00001111	0101111010	0	-1	0101111010	0	1	37	00110111	0111110010	0	-1	0111110010	0	1
10	00010000	1101010010	0	1	1101010010	0	-1	38	00111000	0111000101	2	-1	0111000101	-2	-1
11	00010001	1101010011	2	-1	1101010011	-2	-1	39	00111001	0111000111	2	1	0111000111	-2	1
12	00010010	1101010010	0	-1	1101010010	0	1	3A	00111010	0111001101	2	1	0111001101	-2	1
13	00010011	1101010011	0	1	1101010011	0	-1	3B	00111011	0111001111	2	-1	0111001111	-2	-1
14	00010100	1101110001	2	1	1101110001	-2	1	3C	00111100	0111011001	2	1	0111011001	-2	1
15	00010101	1101110011	2	-1	1101110011	-2	-1	3D	00111101	0111011011	2	-1	0111011011	-2	-1
16	00010110	1101110110	2	-1	1101110110	-2	-1	3E	00111110	0111011110	2	-1	0111011110	-2	-1
17	00010111	1101110010	0	-1	1101110010	0	1	3F	00111111	0111001010	2	-1	0111001010	-2	-1
18	00011000	0101100101	2	-1	1101100101	-2	-1	40	01000000	0100010101	2	1	1100010101	-2	1
19	00011001	0101100111	2	1	1101100111	-2	1	41	01000001	0100010111	2	-1	1100010111	-2	-1
1A	00011010	0101101101	2	1	1101101101	-2	1	42	01000010	0100011101	2	-1	1100011101	-2	-1
1B	00011011	0101101111	2	-1	1101101111	-2	-1	43	01000011	0100011111	2	1	1100011111	-2	1
1C	00011100	0101111001	2	1	1101111001	-2	1	44	01000100	0101010001	2	1	1101010001	-2	1
1D	00011101	0101111011	2	-1	1101111011	-2	-1	45	01000101	0101010011	2	-1	1101010011	-2	-1
1E	00011110	0101111110	2	-1	1101111110	-2	-1	46	01000110	0101010110	2	-1	1101010110	-2	-1
1F	00011111	0101101010	2	-1	1101101010	-2	-1	47	01000111	0100011010	2	1	1100011010	-2	1
20	00100000	0111010101	0	-1	0111010101	0	1	48	01001000	0100110101	2	-1	1100110101	-2	-1
21	00100001	0111010111	0	1	0111010111	0	-1	49	01001001	0100110111	2	1	1100110111	-2	1
22	00100010	0111011101	0	1	0111011101	0	-1	4A	01001010	0100111101	2	1	1100111101	-2	1
23	00100011	0111011111	0	-1	0111011111	0	1	4B	01001011	0100111111	2	-1	1100111111	-2	-1
24	00100100	1111010001	2	1	0111010001	-2	1	4C	01001100	0100101001	2	1	1100101001	-2	1
25	00100101	1111010011	2	-1	0111010011	-2	-1	4D	01001101	0100101011	2	-1	1100101011	-2	-1
26	00100110	1111010110	2	-1	0111010110	-2	-1	4E	01001110	0100101110	2	-1	1100101110	-2	-1
27	00100111	0111011010	0	-1	0111011010	0	1	4F	01001111	0100111010	2	-1	1100111010	-2	-1

NOTES

- 1 The dataword (input) is a fixed-length sequence of bits (8 bits long) prior to conversion.
- 2 The codeword is the result (output) of the 8-10 conversion and is a fixed-length sequence of bits (10 bits long). The codeword is selected by the dataword and Q'.
- 3 Q' is the Q output of the previous codeword.
- 4 Q is the DC information of the codeword.
- 5 The coding direction is from left to right, from MSB to LSB.

Table A.3 (continued) - 8-10 modulation conversion table

Q' = -1								Q' = 1							
Dataword	Codeword	DC	Q	Codeword	DC	Q		Dataword	Codeword	DC	Q	Codeword	DC	Q	
MSB-LSB	MSB - LSB			MSB - LSB				MSB-LSB	MSB - LSB			MSB - LSB			
50	01010000	0100100101	0	-1	0100100101	0	1	80	10000000	1010010101	0	1	1010010101	0	-1
51	01010001	0100100111	0	1	0100100111	0	-1	81	10000001	1010010111	0	-1	1010010111	0	1
52	01010010	0100101101	0	1	0100101101	0	-1	82	10000010	1010011101	0	-1	1010011101	0	1
53	01010011	0100101111	0	-1	0100101111	0	1	83	10000011	1010011111	0	1	1010011111	0	-1
54	01010100	0100111001	0	1	0100111001	0	-1	84	10000100	1010001001	0	-1	1010001001	0	1
55	01010101	0100111011	0	-1	0100111011	0	1	85	10000101	1010001011	0	1	1010001011	0	-1
56	01010110	0100111110	0	-1	0100111110	0	1	86	10000110	1010001110	0	1	1010001110	0	-1
57	01010111	0100101010	0	-1	0100101010	0	1	87	10000111	1010011010	0	1	1010011010	0	-1
58	01011000	0110100101	0	1	0110100101	0	-1	88	10001000	1010110101	0	-1	1010110101	0	1
59	01011001	0110100111	0	-1	0110100111	0	1	89	10001001	1010110111	0	1	1010110111	0	-1
5A	01011010	0110101101	0	-1	0110101101	0	1	8A	10001010	1010111101	0	1	1010111101	0	-1
5B	01011011	0110101111	0	1	0110101111	0	-1	8B	10001011	1010111111	0	-1	1010111111	0	1
5C	01011100	0110111001	0	-1	0110111001	0	1	8C	10001100	1010101001	0	1	1010101001	0	-1
5D	01011101	0110111011	0	1	0110111011	0	-1	8D	10001101	1010101011	0	-1	1010101011	0	1
5E	01011110	0110111110	0	1	0110111110	0	-1	8E	10001110	1010101110	0	-1	1010101110	0	1
5F	01011111	0110101010	0	1	0110101010	0	-1	8F	10001111	1010111010	0	-1	1010111010	0	1
60	01100000	0010010101	0	-1	0010010101	0	1	90	10010000	1100100101	0	1	1100100101	0	-1
61	01100001	0010010111	0	1	0010010111	0	-1	91	10010001	1100100111	0	-1	1100100111	0	1
62	01100010	0010011101	0	1	0010011101	0	-1	92	10010010	1100101101	0	-1	1100101101	0	1
63	01100011	0010011111	0	-1	0010011111	0	1	93	10010011	1100101111	0	1	1100101111	0	-1
64	01100100	1010010001	2	1	0010010001	-2	1	94	10010100	1100111001	0	-1	1100111001	0	1
65	01100101	1010010011	2	-1	0010010011	-2	-1	95	10010101	1100111011	0	1	1100111011	0	-1
66	01100110	1010010110	2	-1	0010010110	-2	-1	96	10010110	1100111110	0	1	1100111110	0	-1
67	01100111	0010011010	0	-1	0010011010	0	1	97	10010111	1100101010	0	1	1100101010	0	-1
68	01101000	0010110101	0	1	0010110101	0	-1	98	10011000	1010100101	2	-1	0010100101	-2	-1
69	01101001	0010110111	0	-1	0010110111	0	1	99	10011001	1010100111	2	1	0010100111	-2	1
6A	01101010	0010111101	0	-1	0010111101	0	1	9A	10011010	1010101101	2	1	0010101101	-2	1
6B	01101011	0010111111	0	1	0010111111	0	-1	9B	10011011	1010101111	2	-1	0010101111	-2	-1
6C	01101100	0010101001	0	-1	0010101001	0	1	9C	10011100	1010111001	2	1	0010111001	-2	1
6D	01101101	0010101011	0	1	0010101011	0	-1	9D	10011101	1010111011	2	-1	0010111011	-2	-1
6E	01101110	0010101110	0	1	0010101110	0	-1	9E	10011110	1010111110	2	-1	0010111110	-2	-1
6F	01101111	0010111010	0	1	0010111010	0	-1	9F	10011111	1010101010	2	-1	0010101010	-2	-1
70	01110000	0010010010	0	1	0010010010	0	-1	A0	10100000	1011010101	2	1	0011010101	-2	1
71	01110001	1011010010	2	-1	0011010010	-2	-1	A1	10100001	1011010111	2	-1	0011010111	-2	-1
72	01110010	1010010010	0	-1	1010010010	0	1	A2	10100010	1011011101	2	-1	0011011101	-2	-1
73	01110011	1010110010	0	1	1010110010	0	-1	A3	10100011	1011011111	2	1	0011011111	-2	1
74	01110100	0010110001	2	1	1010110001	-2	1	A4	10100100	1011001001	2	-1	0011001001	-2	-1
75	01110101	0010110011	2	-1	1010110011	-2	-1	A5	10100101	1011001011	2	1	0011001011	-2	1
76	01110110	0010110110	2	-1	1010110110	-2	-1	A6	10100110	1011001110	2	1	0011001110	-2	1
77	01110111	0010110010	0	-1	0010110010	0	1	A7	10100111	1011011010	2	1	0011011010	-2	1
78	01111000	0011100101	0	1	0011100101	0	-1	A8	10101000	1011110101	2	-1	0011110101	-2	-1
79	01111001	0011100111	0	-1	0011100111	0	1	A9	10101001	1011110111	2	1	0011110111	-2	1
7A	01111010	0011101101	0	-1	0011101101	0	1	AA	10101010	1011111101	2	1	0011111101	-2	1
7B	01111011	0011101111	0	1	0011101111	0	-1	AB	10101011	1011111111	2	-1	0011111111	-2	-1
7C	01111100	0011111001	0	-1	0011111001	0	1	AC	10101100	1011101001	2	1	0011101001	-2	1
7D	01111101	0011111011	0	1	0011111011	0	-1	AD	10101101	1011101011	2	-1	0011101011	-2	-1
7E	01111110	0011111110	0	1	0011111110	0	-1	AE	10101110	1011101110	2	-1	0011101110	-2	-1
7F	01111111	0011101010	0	1	0011101010	0	-1	AF	10101111	1011111010	2	-1	0011111010	-2	-1

Table A.3 (continued) - 8-10 modulation conversion table

Q' = -1				Q' = 1				Q' = -1				Q' = 1			
Dataword	Codeword	DC	Q	Codeword	DC	Q		Dataword	Codeword	DC	Q	Codeword	DC	Q	
MSB-LSB	MSB - LSB			MSB - LSB				MSB-LSB	MSB - LSB			MSB - LSB			
B0	10110000	1101110101	0	1	1101110101	0	-1	D8	11011000	1110100101	0	-1	1110100101	0	1
B1	10110001	1101110111	0	-1	1101110111	0	1	D9	11011001	1110100111	0	1	1110100111	0	-1
B2	10110010	1101111101	0	-1	1101111101	0	1	DA	11011010	1110101101	0	1	1110101101	0	-1
B3	10110011	1101111111	0	1	1101111111	0	-1	DB	11011011	1110101111	0	-1	1110101111	0	1
B4	10110100	1101101001	0	-1	1101101001	0	1	DC	11011100	1110111001	0	1	1110111001	0	-1
B5	10110101	1101101011	0	1	1101101011	0	-1	DD	11011101	1110111011	0	-1	1110111011	0	1
B6	10110110	1101101110	0	1	1101101110	0	-1	DE	11011110	1110111110	0	-1	1110111110	0	1
B7	10110111	1101110101	0	1	1101110101	0	-1	DF	11011111	1110101010	0	-1	1110101010	0	1
B8	10111000	1011100101	0	-1	1011100101	0	1	E0	11100000	1111010101	0	1	1111010101	0	-1
B9	10111001	1011100111	0	1	1011100111	0	-1	E1	11100001	1111010111	0	-1	1111010111	0	1
BA	10111010	1011101101	0	1	1011101101	0	-1	E2	11100010	1111011101	0	-1	1111011101	0	1
BB	10111011	1011101111	0	-1	1011101111	0	1	E3	11100011	1111011111	0	1	1111011111	0	-1
BC	10111100	1011111001	0	1	1011111001	0	-1	E4	11100100	1111001001	0	-1	1111001001	0	1
BD	10111101	1011111011	0	-1	1011111011	0	1	E5	11100101	1111001011	0	1	1111001011	0	-1
BE	10111110	1011111110	0	-1	1011111110	0	1	E6	11100110	1111001110	0	1	1111001110	0	-1
BF	10111111	1011101010	0	-1	1011101010	0	1	E7	11100111	1111011010	0	1	1111011010	0	-1
C0	11000000	1110010101	2	1	0110010101	-2	1	E8	11101000	1111110101	0	-1	1111110101	0	1
C1	11000001	1110010111	2	-1	0110010111	-2	-1	E9	11101001	1111110111	0	1	1111110111	0	-1
C2	11000010	1110011101	2	-1	0110011101	-2	1	EA	11101010	1111111101	0	1	1111111101	0	-1
C3	11000011	1110011111	2	1	0110011111	-2	-1	EB	11101011	1111111111	0	-1	1111111111	0	1
C4	11000100	1110001001	2	-1	0110001001	-2	-1	EC	11101100	1111101001	0	1	1111101001	0	-1
C5	11000101	1110001011	2	1	0110001011	-2	1	ED	11101101	1111101011	0	-1	1111101011	0	1
C6	11000110	1110001110	2	1	0110001110	-2	1	EE	11101110	1111101110	0	-1	1111101110	0	1
C7	11000111	1110011010	2	1	0110011010	-2	1	EF	11101111	1111111010	0	-1	1111111010	0	1
C8	11001000	1110110101	2	-1	0110110101	-2	-1	F0	11110000	1101010101	0	-1	1101010101	0	1
C9	11001001	1110110111	2	1	0110110111	-2	1	F1	11110001	1101010111	0	1	1101010111	0	-1
CA	11001010	1110111101	2	1	0110111101	-2	1	F2	11110010	1101011101	0	1	1101011101	0	-1
CB	11001011	1110111111	2	-1	0110111111	-2	-1	F3	11110011	1101011111	0	-1	1101011111	0	1
CC	11001100	1110101001	2	-1	0110101001	-2	1	F4	11110100	1101001001	0	1	1101001001	0	-1
CD	11001101	1110101011	2	-1	0110101011	-2	-1	F5	11110101	1101001011	0	-1	1101001011	0	1
CE	11001110	1110101110	2	-1	0110101110	-2	-1	F6	11110110	1101001110	0	-1	1101001110	0	1
CF	11001111	1110111010	2	-1	0110111010	-2	-1	F7	11110111	1101011010	0	-1	1101011010	0	1
D0	11010000	1101000101	2	-1	0101000101	-2	-1	F8	11111000	1111100101	2	-1	0111100101	-2	-1
D1	11010001	1101000111	2	1	0101000111	-2	1	F9	11111001	1111100111	2	1	0111100111	-2	1
D2	11010010	1101001101	2	1	0101001101	-2	1	FA	11111010	1111101101	2	1	0111101101	-2	1
D3	11010011	1101001111	2	-1	0101001111	-2	-1	FB	11111011	1111101111	2	-1	0111101111	-2	-1
D4	11010100	1101011001	2	1	0101011001	-2	1	FC	11111100	1111111001	2	1	0111111001	-2	1
D5	11010101	1101011011	2	-1	0101011011	-2	-1	FD	11111101	1111111011	2	-1	0111111011	-2	-1
D6	11010110	1101011110	2	-1	0101011110	-2	-1	FE	11111110	1111111110	2	-1	0111111110	-2	-1
D7	11010111	1101001010	2	-1	0101001010	-2	-1	FF	11111111	1111101010	2	-1	0111101010	-2	-1
Sync									0100010001	0	1	1100010001	0	1	

Annex B

(normative)

MFM/NRZI-RZ modulation codes, PPM recording method

B.1 Scope

This annex defines the logical data structure specific to optical cards using a pulse-position modulation recording method and MFM-RZ and NRZI-RZ modulation codes.

B.2 Definitions

For the purpose of this annex, the following definitions apply:

B.2.1 address: A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination.

B.2.2 BEST code: Burst and random-Error correction-System for- Teletext; a 272,190 majority-logic decodable cyclic error detection and correction code.

B.2.3 code word: The fixed length sequence of bits resulting from encoding a message block using some error detection and correction method.

B.2.4 data area: That portion of the accessible optical area that can be written and/or read under the control of the application software.

B.2.5 error detection code (EDC): A set of code words in which elements conform to specific rules. If errors occur, the resulting presentation will not conform to the rules, indicating that errors are present.

B.2.6 error message: A message returned by a card drive unit to indicate that the card inserted in the drive cannot be processed.

B.2.7 information: The totality of data present on the card including service, system, and user data for interchange independent of the method of recording; that is, whether replicated or written by means of an optical beam.

B.2.8 interleaving: The process of distributing the physical location of code words to render the data more immune to clustered bit errors.

B.2.9 message block: The fixed length sequence of data bits

which is encoded using error detection and correction methods to form a code word.

B.2.10 MFM-RZ: Modified-frequency-modulation-return-to-zero; a specific modulation code also referred to as 1,3 RLL.

B.2.11 NRZI-RZ: Non-return-to-zero-inverted, return to zero. A specific modulation code. NRZI-RZ is similar to MFM-RZ except that a transition does not occur between adjacent zeros.

B.2.12 sector code word: A sector data block encoded using an error detection and correction code.

B.2.13 sector data block: A block of data containing user data and system information.

B.3 First data bit

The first data bit closest the right edge of the card shall be located at 77,4 mm ± 0,7 mm in the x-axis.

B.4 Format structure

This section details information which makes up the accessible optical area and is placed on cards during manufacture and/or at the time of card initialization.

Area	Subsets
Accessible optical area	Guard tracks and data area.
Data area	Format description tracks, test tracks, application description tracks and application area.
Application area	Application data and user data.

B.5 Track layout

Tracks shall be arranged in reverse order beginning with the reference track, the last bottom guard track located nearest the reference edge.

The track layout is outlined below. Because the total number of tracks can vary, the numbers of all tracks located between

the last user data track and the reference track are given in parametric form where n is the nominal number of tracks and $n+9$ is the number of the last bottom guard track, the reference track.

Track description	Track #	Hex
Guard track (last bottom)	$n+9$	
: :	:	
Guard track (first bottom)	n	
Format description track	$n-1$ ¹	
Test track 1 (bottom)	$n-2$ ¹	
: :	:	
Test track 4 (bottom)	$n-5$ ¹	
Application description track	$n-6$ ^{1,2}	
Last user data track	$n-7$ ^{1,2}	
: :	:	
First user data track	6 ^{1,2}	0006
Application description track	5 ^{1,2}	0005
Test track 4 (top)	4 ¹	0004
: :	:	:
Test track 1 (top)	1 ¹	0001
Format description track	0 ¹	0000
Guard track (last top)	-1	3FFF
: :	:	:
Guard track (first top)	-10	3FF6

¹ Data area

² Application area

Tracks shall be numbered in reverse order beginning with the last bottom guard track, the reference track.

B.6 Track layout options

This section provides information concerning data structures that support the optional card layouts described in ISO/IEC 11694-2.

B.6.1 Cards with moderate data capacity

NOTE - These layouts support the inclusion of a magnetic stripe and/or signature panel.

B.6.1.1 Normal density mode

Nominal number of tracks 2 583. This layout shall contain 2 603 data tracks, of which 2 571 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 2592, the reference track.

B.6.1.2 High density mode

Nominal number of tracks 4 144. This layout shall contain 4 164 data tracks, of which 4 132 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 4153, the reference track.

B.6.2 Cards with options, no embossing

NOTE - These layout options support the inclusion of a magnetic stripe, IC chip with contacts, and/or signature panel.

B.6.2.1 Normal density mode

Nominal number of tracks 1 000. This layout shall contain 1 020 data tracks, of which 988 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 1009, the reference track.

B.6.2.2 High density mode

Nominal number of tracks 1 612. This layout shall contain 1 632 data tracks, of which 1 600 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 1621, the reference track.

B.6.3 Cards with options, no IC chip

NOTE - These layouts support the inclusion of a magnetic stripe, embossing, and/or signature panel.

The reference edges for these layouts shall be the top edge and the right edge of the card. See ISO/IEC 11694-2.

For these layouts, the first data bit closest the left edge of the card shall be located at $77,4 \text{ mm} \pm 0,7 \text{ mm}$ in the x-axis.

The track layout for these types of cards shall be displayed from the top to the bottom of the card, beginning with the reference track.

B.6.3.1 Normal density mode

Nominal number of tracks 1 000. This layout shall contain 1 020 data tracks, of which 988 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 1009, the reference track.

B.6.3.2 High density mode

Nominal number of tracks 1 612. This layout shall contain 1 632 data tracks, of which 1 600 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 1621, the reference track.

B.6.4 Cards with maximum data capacity

NOTE - These layouts support the inclusion of a magnetic stripe and/or signature panel.

B.6.4.1 Normal density mode

Nominal number of tracks 3 425. This layout shall contain 3 445 data tracks, of which 3 413 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 3434, the reference track.

B.6.4.2 High density mode

Nominal number of tracks 5 492. This layout shall contain 5 512 data tracks, of which 5 480 shall be user data tracks. Tracks shall be numbered sequentially, in reverse order, beginning with track 5501, the reference track.

B.7 Track guides

The width of the track guides shall be $2,2 \mu\text{m} \pm 0,5 \mu\text{m}$. The distance from the centre of one track guide to the centre of an adjacent track guide shall be $12,0 \mu\text{m} \pm 0,1 \mu\text{m}$ in the normal density mode and $7,5 \mu\text{m} \pm 0,1 \mu\text{m}$ in the high density mode.

A maximum of ten track guides can have breaks exceeding $100 \mu\text{m}$; no breaks shall exceed $500 \mu\text{m}$.

B.8 Guard tracks

Guard tracks -1 to -10 and n to $n+9$ shall contain a copy of the format description track formatted using sector type 13. The 71 excess bytes shall be filled with zeros.

B.9 Format description tracks

There shall be two format description tracks, one located at the top and the other at the bottom of the data area, that shall be preformatted with information that permits the card drive to automatically switch between formats and allows later generations of card formats to be introduced alongside earlier generations. To achieve this upward compatibility, the format description track must be of identical format and location on all generations of card formats.

Format description tracks shall be created when an optical card is manufactured. Card drives shall be unable to write to this track and an optical card shall be deemed invalid unless the format description track is present.

B.9.1 Content

Each format description track shall contain six sectors of 162 bytes. Sectors 0, 2, and 4 shall contain data formats and card manufacturing information; sectors 1, 3, and 5 shall contain

the error message to be returned in case of improper use of the card.

Each format description track shall contain the required fields as described below and as shown in tables B.1 and B.2.

- **data format identifier:** A format identifier unique to each variation in format.
- **track pitch:** The distance from the centre of one track guide to the centre of an adjacent track guide.
- **nominal number of data tracks:** The number of data tracks contained in the data area, expressed in 0,01 mm units.
- **usable track length:** The maximum track length available for written information and preformatted data.
- **type of preformat data:** The method of coding the preformat data.
- **data encoding identifier:** An encoding scheme identifier defining the encoding scheme used.
- **max. sectors per track:** The maximum number of sectors per track allowable.
- **preformatted data bit size:** The nominal size of the preformatted data bits.
- **written data bit size:** The nominal size of the written data bits.
- **written data pitch:** The minimum spacing from the centre of one written bit to the centre of an adjacent written bit.
- **sector type identifier:** An identifier code indicating the type of card sector.
- **EDAC scheme identifier:** An identifier code indicating the EDAC scheme used.
- **media type identifier:** An identifier code indicating the type of media used.
- **card type identifier:** An identifier code indicating the type of card used.
- **manufacturing plant identifier:** An identifier code used to indicate where the card was made.
- **master identifier:** A four character identifier indicating the master used to make the cards.

- **serial number of master:** A four character identifier indicating the serial number of the master used to make the cards.
- **reserved for future use:** Area reserved for future usage.

Fields marked *Std* shall be controlled by the standards body which will assign values and keep a control register of the values assigned. Fields marked *Mfg* shall be assigned values by the individual manufacturers of the cards in cooperation with the card issuer. See tables B.1 and B.2.

B.10 Test tracks

There shall be eight test tracks, four at the top and four at the bottom of the data area, for card drive autodiagnosis and calibration purposes.

B.10.1 Content - Test track 1 (top and bottom)

The first test track shall consist of one sync marker, four leadins, six BOS (see B.13.2), a continuous high frequency pattern (0000) 12 784 bits long, 24 sector padding bits, one sync marker, six BOS and ending with four leadins.

B.10.2 Content - Test track 2 (top and bottom)

The second test track shall consist of one sync marker, four leadins, six BOS, a continuous low frequency pattern (0101) 12 784 bits long, 24 sector padding bits, one sync marker, six BOS and ending with four leadins.

B.10.3 Content - Test track 3 (top and bottom)

The third test track shall consist of one long sector containing random data generated using the generator polynomial defined in B.16.3 according to the following algorithm (x is an unsigned 16-bit number):

- Step 0: If first generated value, set $x=8000$ hex, go to step 4.
- Step 1: Set x to the last generated value.
- Step 2: Shift x by one position to the left, that is, multiply by 2 modulo 2^{16} .
- Step 3: If bit 15 of the last generated value is set, take the bit by bit exclusive OR of x with 1021 hex and put the result in x .
- Step 4: Return x .

The series of random numbers begin with hex 8000, 1021, 2042, 4084, 8108, 1231, 2462, 48C4, 9188, 3331, 6662, CCC4, 89A9, etc...

B.10.4 Content - Test track 4 (top and bottom)

The fourth test track shall consist of 15 type 0 sectors containing incremental data 00, 01, 02, ...FF, 00, 01, 02, ...FF, 00, 01, 02, ...84 hex.

B.11 Application description tracks

Two application description tracks, one at the top and the other at the bottom of the data area, contain a description of the card application along with any error message to be returned if there is a conflict between card and application.

These tracks are optional and can be created either during card manufacture and/or written to the card using an application program. Each application description track shall contain 6 sectors of 162 bytes (sector type 1) or 4 sectors of 233 bytes (sector type 13). If application description tracks are not required, these tracks shall be left blank.

B.12 Data tracks

Each data track can contain a maximum of 69,64 mm of written and/or preformatted data.

B.12.1 Data bits

Written and/or preformatted data bits shall be $2,2 \mu\text{m} \pm 0,5 \mu\text{m}$ in size and the minimum distance from the centre of one data bit to the centre of an adjacent data bit shall be $5,0 \mu\text{m} \pm 0,3 \mu\text{m}$.

B.13 Track components

B.13.1 Auxiliary field

Since the EDAC scheme uses a message block 190 bits long and the sector data consists of an integral number of bytes, bits must be added to form an integral number of message blocks. These additional bits, called auxiliary fields, are processed by the EDAC scheme and are available to the application. The size of the auxiliary field (s_d) can be computed from the number (m) of message blocks contained in the sector:

$$s_d = 190 m \bmod 8$$

NOTE - If m is a multiple of 4, the size of the auxiliary field is zero. Such sectors have no auxiliary fields. See table B.3.

B.13.2 Beginning of sector (BOS)

A series of 48 bits beginning with the track sector address followed by a 4-bit position field which counts the repetition of the BOS, 16 bits of EDC and terminating with a sync

marker. The argument of the EDC polynomial is given by the track sector address and the position field. See figure B.1.

B.13.3 Error detection code (EDC)

A code computed using the generator polynomial found in B.16.3.

B.13.4 Leadin

A series of 48 bits beginning with 40 bits all set to 1 followed by an 8-bit sync marker.

B.13.5 Position field

Four bits which count the repetition of identical BOS data. Counting is done with negative numbers ending at -1 expressed in two's complement. Since data are repeated six times, the position fields contain respectively -6, -5, -4, -3, -2 and -1.

EXAMPLE - (-1) is expressed as 1111 and (-5) as 1011.

B.13.6 Sector padding bits

Continuous zero bits which are added to each sector to make the sector length equal to an integral number of BOS. Since these bits are not processed by the EDAC, they are not available to the application.

B.13.7 Sync marker

A unique 8-bit pattern which cannot be reproduced by any other data using the current modulation code. See figure B.2.

NOTE - When asynchronization occurs during reading, data are resynchronized after sensing successive sync markers.

B.13.8 Data Frame

A 48 bit long data structure containing 40 user data bits and terminated by a sync marker. See figure B.3.

B.13.9 Track sector address (TSA)

A 20-bit long word constructed with the sector address in bits 0 through 5, and the track address in bits 6 through 19. See figure B.4.

B.13.10 Structure of a full track, sector types 0 to 5

A full track shall consist of a preformatted track header, at least one sector, and a termination sequence composed of two leadins minimum (four maximum). The track structure shall be symmetric and shall always be terminated by a sync

marker. See figure B.5.

NOTE - This structure allows tracks to be read in either direction.

B.13.11 Structure of a partially filled track, sector types 0 to 3

A partially filled track shall consist of a preformatted track header and at least one sector of data and shall be terminated by six BOS appearing at the end of the last filled sector. Data added to the track shall be written immediately after the sync marker contained in the last BOS and no gap shall be left between the sync marker and the beginning of the next sector. See figure B.6.

NOTE - This structure allows tracks to be read in either direction.

B.13.12 Structure of a full track, sector types 7 to 15

A track which is filled with maximum interleave sectors, types 7 to 15, shall consist of a preformatted track header, a series of 272 frames, a written track header, and shall be terminated by at least two leadins to allow the track to be read in both directions. The first 40 bits of each frame shall contain the first bits of each sector, and the last 8 bits of each frame shall contain a sync marker. The sector number of the written track header is set to one.

The structure of a track filled with sector types 7 to 15 is shown in figure B.7.

B.13.13 Structure of a partially filled track, sector types 7 to 15

A track which is partially filled with maximum interleave sectors, types 7 to 15, shall be identical to that of a filled track. In case of a track which is partially filled, the bits corresponding to the sectors which have not yet been written are missing in every frame. Sectors with maximum interleave can be written in any order. See figure B.7.

B.14 Track ID

Track ID shall be preformatted at the right side of the data area. All tracks shall be numbered using 20 bits. See figure B.4.

NOTE - The structure allows the track ID to be read from either direction, that is from right to left or left to right.

B.14.1 Preformatted track header

The preformatted track header shall consist of 488 bits beginning with one sync marker followed by two leadins

minimum (four maximum) and six BOS where the sector number of the track sector address is zero.

NOTE - A track is written by scanning the preformatted track header first. A written track can be read in either direction, that is from right to left or left to right.

B.15 Sectors

The type and size of each sector, the respective auxiliary field and the number of padding bits are shown in table B.3.

B.15.1 Sector types 0 to 5

The structure of a sector is shown in figure B.8. Each sector shall consist of:

- User data, auxiliary fields and system data encoded with EDAC (except for type-5) as described in section B.16.3 and B.16.4.
- Sync marker.
- Six BOS containing the address of the sector which follows.

NOTE - Type-5 sectors shall consist of only user data bytes.

B.15.2 Sector types 7 to 15

These sector types shall be written with the maximum possible interleaving factor (48). There shall be one sync marker within each frame and all sync markers shall be written simultaneously at the first write to a track containing these type sectors. For a track containing these types of sectors, the portion located between the two BOS shall consist of 272 frames of 48 bits each. See figure B7.

The frame number i shall consist of a sync marker and 40 bits containing the bit number i of each code word contained in the track. See figure B9.

These sector types are defined by the number m of message blocks which are written within the sector and the interleaving factor used to write the sector. The amount s_d of user data written in a given sector is expressed in bytes as:

$$s_d = \text{floor}(190 m/8) - 4$$

The size s_a of the auxiliary field available for the sector data is expressed in bits as:

$$s_a = 190 m \bmod 8$$

B.15.2.1 Sector type 7

The number of message blocks written in one sector can vary

such that sectors on the same track may have different sizes. However, the sum of the message blocks of all type-7 sectors contained within one full track must be equal to 40.

B.15.2.2 Sector types 8 to 15

The maximum number of sectors per track, n , is obtained from the number m of message blocks as:

$$n = m/40$$

All sectors on a given track shall have the same length.

NOTE - Additional sector types are allowed. However, it is intended that every card drive support at least those sector types specified in table B.3. Applications which use additional sector types must indicate this in the application description track. Using additional sector types may eliminate the possibility of interchange of cards in other card drives.

B.16 Data encoding

This section describes the method for encoding and storing data on optical cards using the various sector types.

B.16.1 Error detection and correction

Two levels of error control shall be applied before data are written to a sector of an optical card. Data shall first be collected into a block containing user data and certain system information. A first level EDC shall be applied to this block to form a sector data block. The sector data block shall be further encoded using an interleaved EDAC coding scheme.

The degree of interleaving shall depend on the sector type. Sector code words, which are generated from sector data blocks, contain data plus parity-check bits which allow the detection of bit-errors and the eventual correction of some of these bit-errors during decoding.

The final code word shall be written to the optical card using a modulation code to represent the binary bits of the code word.

Note: An EDAC coding scheme shall be written, in addition to user data, to all sector types except type-5 which shall be written without EDAC.

B.16.2 Structure of sector data block

B.16.2.1 Length

The length of the sector data block shall be a multiple of 190 bits. The multiple shall depend on the sector type as given in table B.3 and the value shall be equal to the interleaving factor of the EDAC code to be applied later. The block shall be

filled with user data and shall end with the lower 16 bits of the track sector address, the auxiliary field, if any, and 16 bits of EDC resulting from the application to the three items above. See figure B.10.

B.16.2.2 Construction

For all sector types, except type-5 sectors, the sector data block shall be constructed in the following manner:

- The lower 16 bits of the track sector address shall be appended to the user data block, most significant bit first.
- Data shall be divided into 190-bit message blocks with the last block having auxiliary bits added after the track sector address to bring it up to 174 bits; adding 16 bits of EDAC to these 174 bits equals a complete 190-bit message block.
- The first level EDC is calculated across all the 190-bit message blocks with the 16 EDC parity-check bits appended to the last message block after the auxiliary bits, if any, most significant bit first. This makes the last block 190 bits.

B.16.3 First level error detection code

The first level EDC shall be computed using the generator polynomial:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

B.16.4 Second level sector block encoding

The sector data block shall be encoded using the EDAC described in B.16.4.1 to form a sector code word of length $n \times 272$ bits where n is the interleaving factor which is equal to the number of 190-bit message blocks in the sector data block. See figure B.12.

B.16.4.1 Error detection and correction code

Each sector data block shall be encoded using an interleaved code based on the BEST EDAC code generated by the polynomial:

$$g(x) = x^{82} + x^{77} + x^{76} + x^{71} + x^{67} + x^{66} + x^{56} + x^{52} + x^{48} + x^{40} + x^{36} + x^{34} + x^{24} + x^{22} + x^{18} + x^{10} + x^4 + 1$$

The basic code word for a message block of 190 bits has a length of 272 bits and forms the basis for the different interleaved codes used for each sector type as described in B.16.4.2.

B.16.4.2 Interleaving for sector types 0 to 5

The interleaved sector code word for a given sector type shall

be constructed by encoding 190-bit message blocks forming the sector block. The resulting 272-bit code words shall be arranged in a rectangular matrix array, an interleaving frame, with dimensions n rows by 272 columns, where n is the interleaving factor. The value of n will depend on the sector type as given in table B.3. The interleaving frame shall be filled in by row and written to the optical card, column by column, with each column starting at row 1 as shown in figures B.12 and B.13. The code word shall be written to the optical card using MFM-RZ encoding.

B.16.4.3 Type-5 sectors

For type-5 sectors, the sector data block shall consist of only user data bytes. See figure B.11. No track sector address or auxiliary bits shall be added nor shall the first level EDC be applied. The data shall be arranged in 272-bit blocks and interleaved as described in B.16.4.2. See figure B.14.

B.16.4.4 Interleaving for sector types 7 to 15

The interleaved sector code word for a given sector type with maximum interleave is constructed by encoding 190-bit message blocks forming the sector block to obtain 82 parity bits which are appended to the 190 bit message block to form a 272 bit code word. The resulting 272 bit code words are inverted and are placed in a rectangular matrix array, an interleaving frame, with dimensions 40 rows by 272 columns.

The row at which the first message block is placed corresponds to the position of the sector along the track. Unused rows are set to zero.

EXAMPLE - If the second sector of type 9 is written, only rows 3 and 4 will be filled with code words. The remaining rows are filled with zeroes.

The 272 frames are then read and sent to the modulation unit, one column corresponding to one data frame as shown in figure B.15. Data frames are written using the NRZI-RZ encoding which ensures that positions corresponding to the unused rows are not written on the card. If the track is empty, sync markers are written at the end of each data frame. If the track was partially filled, sync markers are not written. Figure B9 shows a frame resulting from the interleaving process.

With the sync marker located at the end of each data frame, a track with sector types 7 to 15 can be read using the MFM-RZ decoding used for sector types 0 to 5.

B.17 Measurement

NOTES

- 1 The reading/writing test conditions outlined in ISO/IEC 11694-3 apply, unless otherwise specified, when observing the optical characteristics.

2 A Nanometrics Nanoline® 4C critical dimension measuring system, or equivalent, with the recommended threshold setting of 35% using the reflected light mode, is used for physical measurements.

B.17.1 Preformatted data measurement

Track pitch, track guide width, and preformatted data bit size shall be measured. The average of a minimum of ten measurements each shall fall within the specified range.

B.17.2 Preformatted data characteristics

The following characteristics shall be achieved when scanning a preformatted portion of the accessible optical area containing high frequency data (5 μm bit pitch), and low frequency data (10 μm bit pitch).

To achieve the expected results, tests shall be conducted using a beam diameter of 2,5 μm and a media linear velocity of 100 mm/s.

B.17.2.1 The low frequency recovery value shall be greater than or equal to 0,7. See ISO/IEC 11694-3.

B.17.2.2 The amplitude comparison value shall be greater than or equal to 0,4. See ISO/IEC 11694-3.

B.17.2.3 The signal overlap (S_o) divided by the high frequency amplitude (A_{HF}) shall be greater than or equal to 0,5. See ISO/IEC 11694-3.

B.17.3 Written data characteristics

The following characteristics shall be achieved when scanning a written portion of the accessible optical area containing high frequency data (6 μm bit pitch), and low frequency data (10 μm bit pitch).

To achieve the expected results, tests shall be conducted using a beam diameter of 3,2 μm and a media linear velocity of 100 mm/s. The write power shall be 6,5 mW and the pulse width shall be 7 μs .

B.17.3.1 The low frequency recovery value shall be greater than or equal to 0,7. See ISO/IEC 11694-3.

B.17.3.2 The amplitude comparison value shall be greater than or equal to 0,4. See ISO/IEC 11694-3.

B.17.3.3 The signal overlap (S_o) divided by the high frequency amplitude (A_{HF}) shall be greater than or equal to 0,5. See ISO/IEC 11694-3.

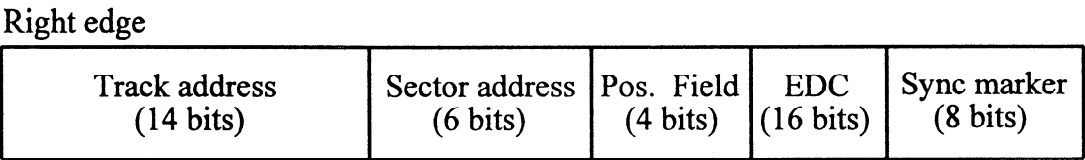


Figure B.1 - Structure of the beginning of sector

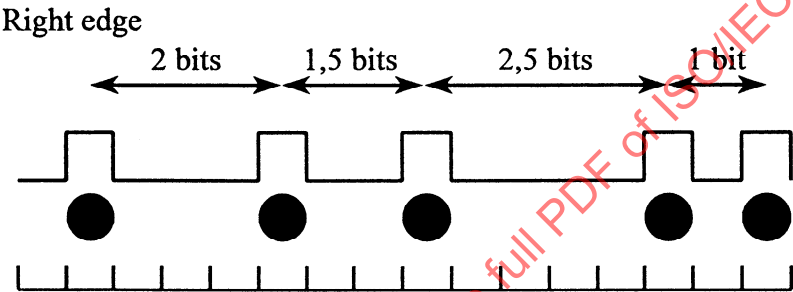


Figure B.2 - Structure of the sync marker

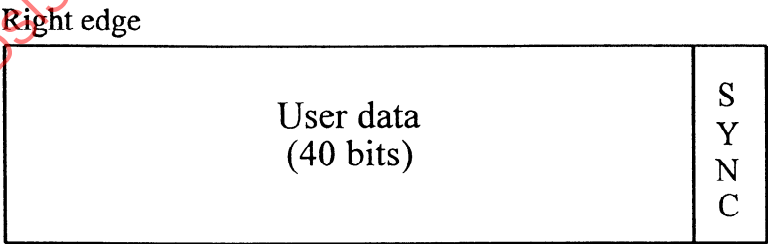


Figure B.3 - Structure of a data frame

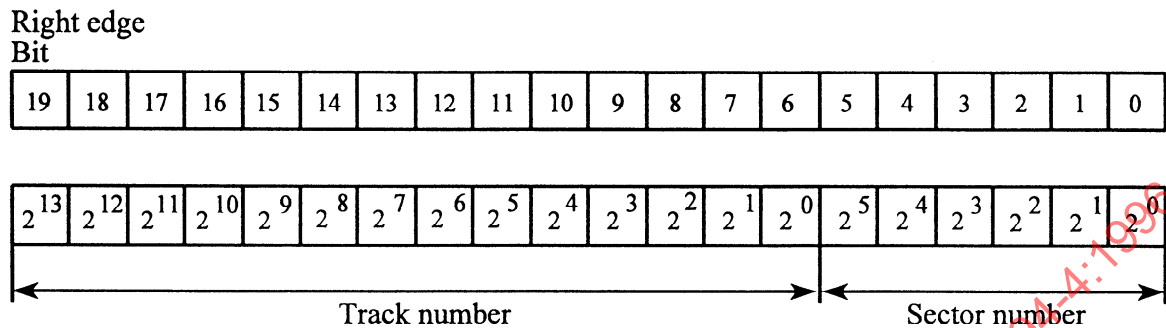


Figure B.4 - Track sector address format

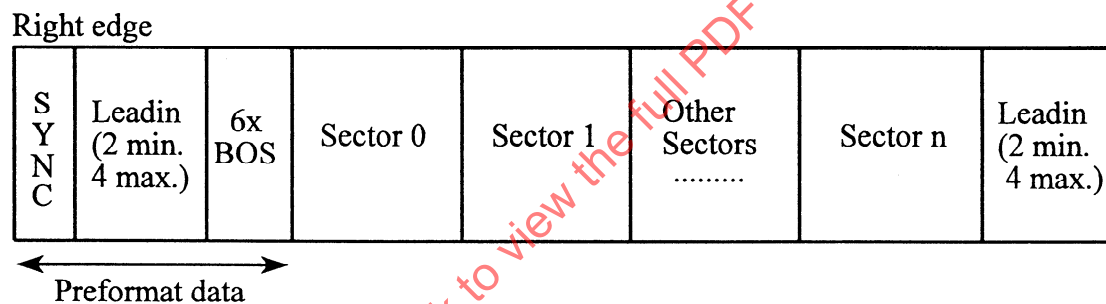


Figure B.5 - Structure of a full track, sector types 0 - 5

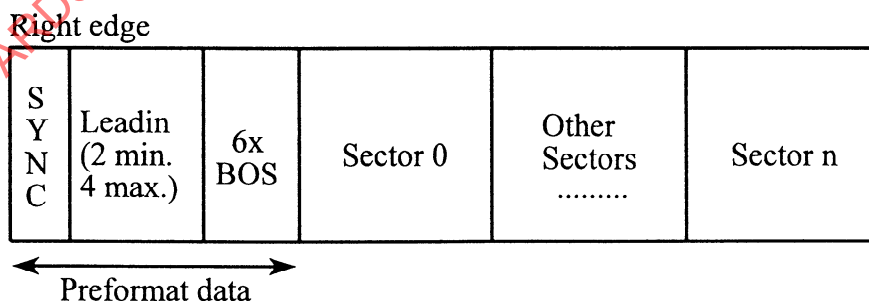


Figure B.6 - Structure of a partially written track, sector types 0 - 3