IEC/TS 62239-1

Edition 1.0 2012-07

TECHNICAL SPECIFICATION

Process management for avionics – Management plan –
Part 1: Preparation and maintenance of an electronic components management plan

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IEC/TS 62239-1:2012(E)

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE XA

ICS 03.100.50; 31.020; 49.060

ISBN 978-2-83220-224-1

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PROCESS MANAGEMENT FOR AVIONICS – MANAGEMENT PLAN –

Part 1: Preparation and maintenance of an electronic components management plan

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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- the required support cannot be obtained for the publication of an International Standard, despite repeated efforts, or
- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC/TS 62239-1, which is a technical specification, has been prepared by IEC Technical Committee 107: Process management for avionics.

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This edition cancels and replaces IEC/TS 62239 published in 2008. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to IEC/TS 62239:2008:

a) Scope – Added DO-254 for clarification
b) Normative references – Added additional references
c) Terms, definitions and abbreviations – Clarified some definitions
d) 4 Technical requirements – Added clarification related to managing ECMP at subcontractor
e) 4.2 Component selection – Clarified temperature range requirements
f) 4.3.3 De-rating and stress analysis – Added information relative to part wear out
g) 4.3.8 Management of lead free termination finish and soldering – Added requirement
h) 4.3.9 Counterfeit, fraudulent and recycled component avoidance – Added requirement
i) 4.4.5 Demonstration of component qualification – Clarified documentation required
j) 4.4.5.3.4 Equipment manufacturer validation – Added additional requirements
k) 4.4.7 Distributor process management approval – Added additional requirements
l) 4.5.2. On-going component quality assurance – Changed title to clarify purpose and changed STACK 0001 reference to IEC/PAS 62686-1
m) 4.6.5 Reporting – Added requirement to periodically report status of obsolescence program to customer
n) 4.6.7 Semiconductor reliability and wear out – Added requirement to address semiconductor wear out
o) Annex A: Typical Qualification Requirements – Added requirement for minimum part qualification
p) Annex B Semiconductor reliability and wear out – Added annex B to provide information about wear out

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
107/161/DTS	107/179/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC/TS 62239 series under the general title *Process management for avionics – Management plan,* can be found on the IEC website.

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The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International Standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

This Technical Specification provides the structure for aerospace equipment manufacturers, subcontractors, maintenance facilities, and other aerospace component users to develop their own Electronic Component Management Plans (ECMPs), hereinafter also referred to as 'plan'. This Technical Specification states objectives to be accomplished; it does not require specific tasks to be performed, specific data to be collected or reports to be issued. Those who prepare plans in compliance with this Technical Specification will document processes that are the most effective and efficient for them in accomplishing the objectives of this Technical Specification. In order to allow flexibility in implementing and updating the documented processes, plan authors are encouraged to refer to their own internal process documents instead of including detailed process documentation within their plans.

Subcontractors or test houses will be assessed by the plan owner on the relevant parts of 4.1 to 4.9 as agreed with the plan owner

This component management Technical Specification is intended for aerospace users of electronic components. This Technical Specification is not intended for use by the manufacturers of electronic components. Components selected and managed according to the requirements of a plan compliant to this Technical Specification may be approved by the concerned parties for the proposed application, and for other applications with equal or less severe requirements.

Organizations that prepare such plans may prepare a single plan, and use it for all relevant products supplied by the organization, or may prepare a separate plan for each relevant product or customer.

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PROCESS MANAGEMENT FOR AVIONICS – MANAGEMENT PLAN –

Part 1: Preparation and maintenance of an electronic components management plan

1 Scope

This part of the IEC/TS 62239 series defines the requirements for developing an Electronic Components Management Plan (ECMP) to assure customers and regulatory agencies that all of the electronic components in the equipment of the plan owner are selected and applied in controlled processes compatible with the end application and that the technical requirements detailed in Clause 4 are accomplished. In general, the owners of a complete electronic components management plan are avionics equipment manufacturers. This part of the IEC/TS 62239 series provides the minimum requirements for system development assurance levels according to levels A, B and C of the DO-254 A, B and C for flight equipment.

Although developed for the avionics industry, this process may be applied by other industrial sectors.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

IEC/TR 61340-5-2, *Electrostatics – Part 5-2: Protection of electronic devices from electrostatic phenomena – User guide*

IEC/TR 62240, *Process management for avionics – Use of semiconductor devices outside manufacturers' specified temperature range*

IEC 62396-1, *Process management for avionics – Atmospheric radiation effects – Part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment*

IEC/TS 62396-2, *Process management for avionics – Atmospheric radiation effects – Part 2: Guidelines for single event effects testing for avionics systems*

IEC/TS 62396-3, *Process management for avionics – Atmospheric radiation effects – Part 3: Optimising system design to accommodate the single event effects (SEE) of atmospheric radiation*

IEC/TS 62396-4, *Process management for avionics – Atmospheric radiation effects – Part 4: Guidelines for designing with high voltage aircraft electronics and potential single event effects*

IEC/TS 62396-5, *Process management for avionics – Atmospheric radiation effects – Part 5: Guidelines for assessing thermal neutron fluxes and effects in avionics systems*

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IEC 62402, *Obsolescence management – Application guide*

IEC/TS 62564-1, *Process management for avionics Aerospace qualified electronic components (AQEC) – Part 1: Integrated circuits and discrete semiconductors*

IEC/PAS 62647-1, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 1: Lead-free management*

IEC/TS 62647-1[1], *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 1: Preparation for a lead-free control plan*

IEC/PAS 62647-2, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 2: Mitigation of the deleterious effects of tin*

IEC/TS 62647-2[2], *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 2: Mitigation of the deleterious effects of tin*

IEC/TS 62668-1, *Process management for avionics – Counterfeit prevention – Part 1: Avoiding the use of counterfeit, fraudulent and recycled electronic components*

IEC/PAS 62686-1, *Process management for avionics – Aerospace qualified electronic components (AQEC) – Part 1: General requirements for high reliability integrated circuits and discrete semiconductors*

IEC/TS 62686-1[3], *Process management for avionics – Aerospace qualified electronic components (AQEC) – Part 1: General requirements for high reliability integrated circuits and discrete semiconductors*

ISO 9000:2005, *Quality management systems – Fundamentals and vocabulary*

JEP 149:2004, JEDEC Standard, *Application Thermal Derating Methodologies*

JESD 47, JEDEC Standard, *Stress – Test-driven qualification of integrated circuits*

JESD 94.01, JEDEC Standard, *Application Specific Qualification Using Knowledge Based Test Methodology*

MIL-HDBK-263, Revision B, *Electrostatic Discharge Control Handbook*

AEC–Q100, *Failure Mechanism based Stress Test Qualification for Integrated Circuits*

AEC–Q101, *Stress Test Qualification for Automotive Grade Discrete Semiconductors*

AEC–Q200, *Stress Test Qualification for Passive components*

SAE AS5553, *Counterfeit Electronic Parts, Avoidance, Detection, Mitigation, and Disposition*

ANSI/GEIA-STD-0002-1, *Aerospace Qualified Electronic Component (AQEC) Volume 1 – Integrated Circuits and Semiconductors*

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1 To be published. This will supersede the PAS document.

2 To be published. This will supersede the PAS document.

3 To be published. This will supersede the PAS document.

ANSI/GEIA-STD-0005-1, *Performance Standard for Aerospace and Military Electronic Systems Containing Lead-Free Solder*

ANSI/GEIA-STD-0005-2, *Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems*

GIFAS/5052/2008, *Guide for managing electronic component sourcing through non franchised distributors. Preventing fraud and counterfeiting*

AS/EN/JISQ *9100 Quality Management Systems-Requirements for Aviation Space and Defense Organizations*

IPC/JEDEC J-STD-20*, Moisture/Reflow Sensitivity Classifications*

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3 Terms, definitions and abbreviations

For the purposes of this document, the following terms, definitions and abbreviations apply.

In their plan, plan owners may use alternative definitions consistent with convention in their company.

3.1 Terms and definitions

3.1.1
environment
applicable environmental conditions (as described per the equipment specification) that the equipment is able to withstand without loss or degradation in equipment performance throughout its manufacturing cycle and maintenance life (the length of which is defined by the equipment manufacturer in conjunction with customers)

3.1.2
purchased
bought outside the plan owner organization, from an independent supplier

Note 1 to entry: This indicates that the plan owner does not manufacture this in-house

3.1.3
capable
capacity of a component to be used successfully in the intended application

3.1.4
certified
assessed and compliant to an applicable 3rd party

3.1.5
characterization
process of testing a sample of components to determine the key electrical parameter values that can be expected of all produced components of the type tested

3.1.6
component application
domain of use where the component meets the design requirements

3.1.7
component manufacturer
organization responsible for the component specification and its production

3.1.8
component obsolescence
absence of availability of a component which is not procurable due to the manufacturer(s) ceasing production

Note 1 to entry: Component obsolescence management is considered as an element of component dependability

3.1.9
component qualification
process used to demonstrate that the component is capable of meeting its specification for all the required conditions and environments

3.1.10
component quality assurance
activities and processes to provide adequate confidence that each individual component meets the performance and environmental requirements

3.1.11
component selection
process of choosing a specific component for a specific application

3.1.12
component standardization
process of developing and agreeing by consensus on uniform engineering criteria for products and methods for achieving compatibility, interoperability, interchangeability, or commonality of material

Note 1 to entry: Standardization is used to reduce proliferation of parts into inventory.

3.1.13
counterfeit
practice of producing products which are imitations or are fake goods or services and, therefore, infringes the intellectual property rights of the original manufacturer.

Note 1 to entry: Counterfeiting is illegal and generally relates to wilful trade mark infringement

3.1.14
fraudulent
produced or distributed in violation of the law

EXAMPLE Fraudulent parts include but are not limited to:

a) parts which do not contain the proper internal construction (die, manufacturer, wire bonding etc.),

b) parts which have been used refurbished or reclaimed but represented as new product,

c) parts which have different package style or surface plating/finish than the ordered parts,

d) parts which have not successfully completed the original component manufacturer's full production and test flow but are represented as the completed product,

e) parts sold as upscreened parts which have not successfully completed upscreening,

f) parts sold with modified labelling or markings intended to misrepresent the part's form, fit, function or grade,

g) parts which have been refinished, upscreened or uprated and have been identified as such, and are submitted as compliant parts, are not considered fraudulent (SAE AS5553, IEC/TS 62668-1:2012, definition),

h) pieces rejected at manufacturing level which meet the definition of a counterfeit part.

Note 1 to entry: This includes stolen electronic components, components scrapped by the original component manufacturer or by any user, disassembled components salvaged and resold as new components, counterfeit components, copies, imitations, full or partial substitutes of brands, designs, models, patents, software or copyright for example: components whose production and distribution are not controlled by the original manufacturer, unlicensed copies of a design, disguised components (remarking of the original manufacturer name, reference date/code or other identifiers etc.) components without chips or chips other than of the original manufacturers' chips.

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3.1.15
dependability
capability of a product enabling it to achieve the specified functional performance at the appropriate time and for the planned duration, without damage to itself or its environment

Note 1 to entry: Dependability is generally characterised by the following four parameters: reliability, maintainability, availability, safety.

3.1.16
franchised distributor
individual or organization that is legally independent from the franchiser (in this case the electronic component manufacturer or OCM) and who agrees under contract to distribute products under the franchiser's name and sales network

3.1.17
Electronic Components Management Plan
ECMP
equipment manufacturer's document that defines the processes and practices for applying components to an equipment or range of equipment and which generally addresses all relevant aspects of controlling components during system design, development, production, and post-production support

3.1.18
electronic components
electronic parts
piece parts
electrical or electronic devices that are not subject to disassembly without destruction or impairment of design use.

EXAMPLE Resistors, capacitors, diodes, integrated circuits, hybrids, application specific integrated circuits, wound components and relays.

3.1.19
electronic equipment
functioning electronic device produced by the plan owner, which incorporates electronic components

EXAMPLE End items, sub-assemblies, line-replaceable units and shop-replaceable units.

3.1.20
flight equipment
equipment used for the active flying of the aircraft (UAV etc.) and associated with active flying of the aircraft such as flight recorders, etc.

Note 1 to entry: This excludes equipment fitted to the aircraft not actively involved with the flying of the aircraft, such as in-flight entertainment, galley equipment, etc.

3.1.21
may
indicates a course of action which is permissible within the limits of this Technical Specification

3.1.22
obsolete component
component which is no longer manufactured, and may or may not still be available

3.1.23
package type
generic package family describing the physical outline and lead style

EXAMPLE Plastic quad flat-package, ball grid array, chip scale package, SOIC package, SOT23, etc.

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3.1.24
plan owner
original design authority responsible for all aspects of the design, functionality and reliability of the delivered equipment in the intended application and is responsible for writing and maintaining their specific ECMP

3.1.25
risk
measure of the potential inability to achieve overall program objectives within defined cost, schedule, and technical constraints

3.1.26
risk management
act or practice of dealing with risk that includes planning for risk, assessing (identifying and analysing) risk areas, developing risk handling options, monitoring risks to determine how risks have changed, and documenting the overall risk management program

3.1.27
shall
indicates a requirement

3.1.28
should
indicates that, among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is discouraged but not prohibited

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3.1.29
single event effect
response of a component caused by the impact of galactic cosmic rays, solar enhanced particles and/or energetic neutrons and protons

Note 1 to entry: The range of responses can include both non-destructive (for example upset) and destructive (for example latch-up or gate rupture) phenomena.

3.1.30
subcontractor assembly facilities
location where subcontractor conducts assembly processes and uses approved test equipment to the plan owners drawings and bills of material and test specifications without owning the intellectual property rights to the equipment

3.1.31
subcontractor
person or entity to whom the holder of obligations under a contract has delegated part or all of such obligations

3.1.32
substitute component
component used as a replacement in equipment after the equipment design has been approved

Note 1 to entry: In some contexts, the term “alternate component” is used to describe a substitute component that is equal to or better than the original component.

3.1.33
validation
method of qualifying components at the equipment manufacturer, when no in service data from prior use is available and there is no manufacturer’s qualification data to analyse

3.2 Abbreviations

AQEC Aerospace Qualified Electronic Component (see IEC 62564-1)

COTS Commercial Off The Shelf

DSCC Defence Supply Centre Columbus

ECMP Electronic Components Management Plan

EMC Electromagnetic Compatibility

ESS Environmental Stress Screening

IECQ International Electrotechnical System Quality

NSI National Supervising Inspectorate

OEM Original Equipment Manufacturer

OCM Original Component Manufacturer

PCN Part Change Notice

UAV Unmanned Avionic Vehicle

4 Technical requirements

4.1 General

The plan shall document the processes used by the plan owner to accomplish the following requirements. These requirements shall apply to all electronic components, including off-the-shelf components, which are defined by the component manufacturer's data sheet, and custom components, which are defined by the original equipment manufacturer:

a) component selection;
b) component application;
c) component qualification;
d) component quality assurance;
e) component dependability;
f) component compatibility with the equipment manufacturing process;
g) component data;
h) configuration control.

The plan shall state clearly, concisely, and unambiguously:

- what the plan owner does to accomplish each of the requirements;
- how compliance to the plan is demonstrated; and
- the evidence that is available to show that the requirements have been accomplished.

The plan shall document the processes used to address each of the requirements listed above and described in 4.1 to 4.9 depending on program or product line requirements and the plan owner may, with appropriate justification, amend the above list of requirements by adding or deleting requirements. If this is done, then the plan shall be assessed according to the amended list of requirements stated in the plan.

The only type of amendment permitted is to add or delete entire requirements (those designated and described in 4.1 to 4.9). Modification of any of the requirements listed above and described in this clause is not permitted.

All the requirements given in this clause apply to equipment as stated in 5.6. The above requirements may be satisfied by either the Original Equipment Manufacturer (OEM plan owner) or may be subcontracted. In either case, the OEM shall satisfy and demonstrate compliance to all requirements.

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If part or all of the equipment design/manufacturing is designed or manufactured by a subcontractor, the plan owner shall document how the subcontractor is managed, maintaining compliance with the applicable clauses of IEC/TS 62239-1.

Table C.1 provides guidelines for environmental protection techniques to be considered during the avionics design process.

Ground support test equipment, flight demonstrator assemblies, and prototypes are typically exempt from these requirements, unless the plan owner states otherwise in their plan (see 5.6).

The plan shall satisfy the requirements of this clause with objective evidence, regardless of the source from which the plan owner obtains components.

NOTE

– An ECMP plan can be certified by an international third party organization like IECQ (or other).
– Subcontractors' ECMP plan can be audited by the OEM and/or his customer. Information regarding skills of the auditor and his training can be found, for example, in applicable sections of IECQ documents: IECQ 03-4, IECQ OD 702 and IECQ OD 703.
– The supplier can get objective evidence that the subcontractors products satisfies the requirements of IEC/TS 62239-1, according to tests or analyses conducted by either the supplier or the subcontractor, and approved by the customer.

4.2 Component selection

All components shall be selected according to documented processes and shall satisfy the requirements of this subclause regardless of additional criteria such as standardisation, order of preference, etc. The termination finish of all components shall be identified and the risk of any lead-free finishes assessed (see 4.3.8).

Because of the highly individual nature of most plan owners' administrative processes, no detail is included here. Component selection can include the use of a preferred COTS component list, provided the requirements of this subclause are met when the components are placed onto the standard list. Components should then be selected from the standard list for use in specific applications. The selection process may include levels of preference. This may refer to another process document describing how parts are selected. A preference list can be included in a contract document.

It is recommended that component selection utilizes the following criteria:

– number of component types be minimised;
– components be selected from those readily available and produced in large volume;
– components be selected from those in a preferred stage of their lifecycle.

The conditions for use of the component shall be adequately identified, from the component specification based on the component manufacturer's data sheet and any additional requirements to ensure suitability in the end application.

Availability and level of obsolescence risk should be considered as major component selection criteria.

Components shall be selected within temperature ranges in excess or matching the temperature range required in the application, see 4.3.4.

Components which meet the requirements of IEC/PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 need to be applied in avionics applications with caution as they may not necessarily meet the full requirements of 4.3 (component application) and 4.6 (component availability and associated risk assessment). In some applications an AQEC component in conformity with IEC/TS 62564-1 or custom component with special design

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characteristics or special screening may be required instead. Users need to demonstrate why IEC/PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 components can be successfully used in avionics applications. Such demonstrations may include (1) the analysis of component field history of similar equipment in similar avionics applications, (2) unit qualification testing of similar equipment, (3) component qualification testing, (4) other analysis etc.

The use of AQEC components to IEC/TS 62564-1 or GEIA-STD-0002-1 (see 4.4.5.3.1) may be considered where there are no off-the-shelf components available which will operate within the temperature limits required.

If additional performance is required (for example upscreening, uprating, additional parameters defined), then the component shall be considered as a specific one and shall be uniquely identified. (See thermal analysis, 4.3.4.)

Each selected component shall be comprehensively identified within the selection process.

- For off-the-shelf components, as a minimum, the component manufacturer's data sheet, technical and application notes, packaging, reliability and availability data, productibility data (including storage, soldering conditions, etc.), lead-free status and lead-free termination finish shall be identified.
- For components specified by the equipment manufacturer, the specific documentation (including specification, manufacturer data and process, reliability, specific tests and screening, and associated in-house continuous monitoring) shall be identified.

4.3 Component application

4.3.1 General

Listed here are some categories of component application processes that may be documented in a plan. Not all of the categories listed below are relevant to every component application; therefore, the requirements listed below are applicable only if relevant to the given application. The plan shall document the processes that are expected to be applicable to the majority of the plan owner's products, with the understanding that some of the documented processes may not be used for specific programs or specific functionality of products.

In each case, the documented processes shall verify if the equipment containing the component shall continue to meet its performance requirements and specifications throughout the manufacturing, full service storage, and operating lifetime. In order to determine design suitability of equipment, there shall be a formal design review. At the design review, consideration for each component shall be given to all design aspects including those given in 4.3.7 to 4.3.9.

The following application processes are not specific to an individual component, but are typically encountered when the component is placed into a circuit assembly.

A documented report shall be prepared against each of the following design aspects:

4.3.2 Electromagnetic compatibility (EMC)

EMC is demonstrated by analysis, testing and simulation to customer requirements. The component performance shall be capable of EMC compliance at equipment level.

Certain components, for example high power switching components, may produce more electromagnetic signal than other types and additionally certain components can be more susceptible to electromagnetic interference than others. Component level EMC aspects have been addressed in IEC 61967-1. Testing is typically carried out at electronic equipment level.

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4.3.3 Derating and stress analysis

The documented processes shall verify that the component is used within the operating limits specified by the component manufacturer per a documented set of derating criteria.

When the component manufacturer provides derating criteria and methods, they shall be used where applicable. If the component manufacturer does not provide this information, or if it is not applicable, then the plan owner shall develop and document appropriate derating criteria and methods. All instances in which a component is not used within the limits defined above shall be documented in the design records. In all such instances, either corrective action shall be taken, or justification for not satisfying the criteria shall be documented.

Derating methods that can be used in avionics applications can be found in JEP149. Components handled in the manner described in JEP149 are considered to be used within the specification limits provided by the manufacturer, if internal parameters and technical data used for component thermal modelling (which ensures the application) are documented with the component manufacturer data. JEP149 outlines two important analyses related to thermal considerations of the application: reliability and functional performance, both of which employ a process utilizing junction temperature analysis. These analyses may require information from the component manufacturer not provided in published data sheets. In these cases, the manufacturer shall be contacted to determine the data needed to support appropriate application of the part with regard to these issues.

NOTE Derating the device stressors can mitigate for semiconductor wear out mechanisms (see 4.6.7) and could enable improvement of both the device reliability and the device operating life capability. The derating can take several forms which include voltage derating, operating frequency reduction, part held in standby till required reduction of power dissipated and environment improvement. Methods of thermal derating of semiconductor devices are detailed in JEP149 and methods for determining acceleration factors form testing detailed in JESD91A.

See Annex B for more information.

4.3.4 Thermal analysis

The documented processes shall verify that the component is used within the temperature limits specified by the component manufacturer, or by the plan owner.

Where there are no off-the shelf components which are functionally appropriate and which operate with the temperature limits specified, the use of AQEC components (see 4.4.5.3.1) to IEC/TS-62564-1 or GEIA-STD-0002-1, with wider temperature range may be considered.

If components are used outside the temperature ranges specified by the component manufacturer, then the supplier shall demonstrate how he controls this process. Recommendations and guidelines on how to do this are contained in IEC/TR 62240 and may be used in addition to the plan prepared according to this Technical Specification. Note that use of IEC/TR 62240 is a non-preferred technique. Equivalent procedures from other documents may also be acceptable.

NOTE 1 A common maximum temperature for semiconductor devices is the junction temperature. In some instances, other limiting temperatures may be specified for semiconductor devices driven by physical properties of materials used in packaging, bond pad and lead frame, etc., and other types of components. When the application thermal analysis has successfully implemented the thermal and stress analysis process outlined in 4.3.3, in accordance with the component manufacturer, the component is considered to be used within the manufacturer's rating.

NOTE 2 In some instances, the manufacturer may not specify the maximum temperature. However, the maximum temperature may be calculated from other information supplied by the component manufacturer.

NOTE 3 Verification processes may include analysis, modelling, thermal survey, simulation, or testing. Testing is typically carried out at electronic equipment level.

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4.3.5 Mechanical analysis

The documented processes shall verify that the component is mechanically compatible with the application. This includes mechanical fit, as well as the ability to withstand vibration, mechanical shock, and mechanical stresses including those generated by mismatches of coefficients of thermal expansion of the different materials.

NOTE Verification processes may include analysis, modelling, simulation, or testing.

4.3.6 Testing, testability, and maintainability

The documented processes shall assure testability and maintainability of the equipment by the plan owner.

The focus here is on testing and testability with regard to component verification, not on software or system verification. Examples include board level or sub-assembly level testing, provision for test pins, and that other equipment level tests will be available to verify component function at the appropriate level. Exhaustive testing of complex components is not always realistic, but documented processes should assure some level of evaluation of all components at appropriate points in the production flow.

This requirement also includes design for maintainability, for example, placement for ease of component replacement, mounting that minimises the risk of damage during maintenance and assures equipment quality following maintenance or repair by equipment manufacturer.

4.3.7 Avionics radiation environment

The documented processes shall verify that the components will operate successfully in the application with regard to the effects of atmospheric radiation on them. These include various types of single event effects (SEE), such as single event upset (SEU), single event latch-up (SEL), single event burn-out (SEB) and single event functional interrupt (SEFI). If radiation effects are accommodated by the equipment design, then the method of accommodation shall be documented in the equipment design records. Guidance on the effects of atmospheric radiation may be found in the IEC 62396 series. The effects of atmospheric radiation and their accommodation shall be assessed and documented in accordance with the SEE compliance Clause 9 of IEC 62396-1:2012 and with reference to the other parts of the IEC 62396 series.

The SEE assessment is achieved through quantifying the SEE rates in avionics systems in accordance with IEC 62396-1, based on:

a) the atmospheric neutron environment;

b) the components in a given system;

c) the SEE response of those components to energetic neutrons.

NOTE The SEE response of devices is complicated and has been shown to increase significantly with advancing integrated circuit technologies, e.g., reduced feature size. Thus for feature sizes of < 35 nm in SRAMs, all neutron interactions are expected to result in two or more upsets within the memory array compared to technologies of >150 nm where approximately 3 % to 5 % of the interactions resulted in multi-cell upsets. In a similar manner different revisions of the same component (identical part number) incorporating modifications in their die fabrication process, can dramatically change from no sensitivity to a pronounced SEE sensitivity.

4.3.8 Management of lead-free termination finish and soldering

The OEM shall document a lead-free control plan in accordance with IEC/PAS 62647-1 (GEIA-STD-0005-1) or IEC/TS 62647-1 that will supersede IEC/PAS 62647-1 and IEC/PAS 62647-2 (GEIA STD-0005-2) or IEC/TS 62647-2 that will supersede IEC/PAS 62647-2.

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4.3.9 Counterfeit, fraudulent and recycled component avoidance

IEC/TS 62668-1 gives guidelines to assist with avoiding counterfeit, fraudulent and recycled components.

The OEM shall have a counterfeit, fraudulent and recycled component risk mitigation plan based on industry documents like SAE AS5553 and/or GIFAS/5052/2008.

4.4 Component qualification

4.4.1 General

The documented processes shall verify that the installed component is qualified for the application requirements for performance and reliability through the processes listed in this Technical Specification.

Annex A provides guidance for typical component minimum qualification requirements which may be applicable.

Table C.1 provides guidelines for environmental protection techniques to be considered during the avionics design process.

Table C.2 provides guidelines for the comparison of internationally available component specifications for microcircuits.

The tables in the annex shall be used with caution. The avionics OEM shall be responsible for ensuring components selected using Annex A meet the application requirements. The avionics OEM may need to carry out additional testing, analysis, further verification etc., as needed to ensure all application requirements are accommodated (see 4.3).

4.4.2 General component qualification requirements

Components shall be obtained from manufacturers who meet the requirements of 4.4.3, 4.4.4, and 4.4.5; or alternatively, the requirements of 4.4.6 shall apply.

4.4.3 Component manufacturer quality management

4.4.3.1 Quality system

The component manufacturer shall have a quality system assessed to the relevant parts of the ISO 9000 series or equivalent. The documented quality management system is a major part of the plan owner verification.

4.4.3.2 Quality system assessment

Where the component manufacturer is not assessed in accordance with 4.4.3.1 above or an approved existing scheme, then the plan owner shall demonstrate how the quality management system of the component manufacturer shall be maintained. Where the plan owner conducts or enables an audit on the component manufacturing facility, then the audit shall be conducted by suitably trained auditors in accordance with the relevant standards of the ISO 9000 series or equivalent system.

4.4.4 Component manufacturer process management approval

The plan owner shall verify that the component manufacturer has a manufacturing process capability utilising manufacturing technologies with demonstrable repeatability.

This may be satisfied by one of the following.

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a) Approval of the component manufacturing process by a third party, or within an international second party system with specific verification that the manufacturing process results in demonstrated product repeatability.

b) Where the component manufacturer is not assessed as in a) above, then the plan owner shall demonstrate how the process management capability of the component manufacturer is ensured. When the plan owner conducts or enables an audit on the component manufacturing facility, then the audit shall be conducted by suitably trained auditors (as in 4.4.3.2 above).

4.4.5 Demonstration of component qualification

4.4.5.1 General

The plan owner shall document the component qualification process for each component.

The documented processes shall verify that the installed component is qualified for the circuit application requirements for performance and reliability through the processes listed in this Technical Specification.

The qualification plan and test procedures, sampling and criteria of acceptance (with the defined margins) shall be documented. The approach to quality and reliability required in the application shall be documented.

This can be demonstrated by any of the following, but the choice shall be justified.

4.4.5.2 Component qualification by an external party

Components qualified in accordance with a second or third party approval system as in 4.4.4, a) with documented evidence that the qualification is appropriate for the application.

4.4.5.3 Component qualification by the equipment manufacturer

4.4.5.3.1 Component manufacturer technology qualification data

Component qualification by the equipment manufacturer can be demonstrated by one or more of the following subclauses 4.4.5.3.1 to 4.4.5.3.4. Component manufacturers perform and record data from initial and regular on-going qualification testing on significant numbers of components. The plan owner shall review such defined qualification testing with acceptance criteria and resulting data for suitability in the end application. Component manufacturers produce components across a wide range of market sectors, and qualification testing will reflect these. Stress levels in the component qualification should equate to or exceed those of the end application or additional testing will be necessary. This data is not guaranteed performance data and the avionics manufacturer shall validate that each device type utilized is adequately qualified for the customer performance requirements.

The component manufacturer may choose to qualify specific components in accordance with JESD94, JESD47, AEC-Q100, AEC-Q101 and/or AEC-Q200. If the use of JESD94 is determined to be applicable to any parts to be used on an avionics application, it shall be specifically demonstrated that the manufacturer's qualification data was applicable to the avionics application.

The integrated circuit manufacturers are increasingly limiting their products to commercial or industrial temperature range products. This trend is most pronounced in the functional areas that are critical to avionics products, microprocessors, FPGA's and memories.

The use of data obtained from an avionics qualified electronic component manufacturer (as per IEC/TS 62564-1 or GEIA-STD-0002-1) is permitted and encouraged. This data is not guaranteed performance data and it will be necessary for the avionics manufacturer to validate that each device utilized meets the customer performance requirements in 4.3, 4.4 and 4.6.

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NOTE Components compliant to AQEC are typically sole source products. Further, each AQEC device type may be tested to different levels, therefore there is no standardization guaranteed from one AQEC manufacturer to another for the same nominal part.

The AQEC program is basically a mechanism to obtain data from the device manufacturer which is not formally available. The availability of this data does not substitute for guaranteed performance data and device characteristic changes are not necessarily going to be covered by PCN's or other change notification.

4.4.5.3.2 In-service experience

Satisfactory performance including reliability of the component in a similar or harsher environment shall be documented.

4.4.5.3.3 Similarity

Documentary evidence from test data or in-service experience of a previously qualified associated component shall be given. The plan shall address the ground rules for assessment by similarity to other component. For further details on similarity rules, refer to relevant standards.

NOTE For example AEC-Q100/101/200.

4.4.5.3.4 Equipment manufacturer validation

Validation may be employed particularly if components are from a manufacturer, component technology or package type not previously used before.

The plan owner may need to perform component qualification at component level, with completion at equipment level, for new technologies or package types not used before. New components can be qualification tested within the equipment assembly, without complete testing at the component level.

Component qualification with tests at equipment level shall be documented and used only when none of the other methods specified are acceptable.

For those equipment which contain software, component qualification shall demonstrate or verify that the component and the operational software are compatible over the entire operating range of the equipment.

There shall be suitable, defined and justified margins utilized for this demonstration of component qualification to validate that component variations will not cause equipment failure during operation.

If equipment manufacturer validation is utilized because the component qualification information available does not support use of the component in the application, a suitable final acceptance test for each end product shall be done with defined and justified margins.

4.4.6 Qualification of components from a supplier that is not qualified

If the component supplier is not qualified, then the plan shall document how the components are qualified.

4.4.7 Distributor process management approval

The plan owner shall verify that the distributors have a documented quality management system.

The distributor quality management system shall be assessed according to 4.4.3.1 or 4.4.3.2 and applicable to distributors. The distributor shall have an ISO 9000 series or equivalent

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approved process management system for all its activities including storage, component handling, traceability, testing, shipment, information and technical data handling.

If the distributor supplies parts other than from a manufacturer franchise then the distributor shall have a process for counterfeit electronic parts avoidance.

When the distributor accepts returned stock from customers, these parts will have to be considered in the counterfeit/fraudulent management risk plan.

NOTE 1 IEC/TS 62668-2 is currently under consideration to offer guidelines for managing non franchised distributors.

NOTE 2 Examples of such processes are the development and implementation of a component qualification process conducted by the plan owner, the component distributor, component manufacturer or a third party.

4.4.8 Subcontractor assembly facility quality and process management approval

The plan owner shall verify that all subcontract assembly facilities have a documented quality management system in accordance with AS/EN/JISQ 9100 or equivalent, where specific attention is made to the following requirements for avionics plan owners:

1) Component traceability is maintained to the original manufacturer.
2) Component substitutions shall be approved by the plan owner.
3) The requirements of 4.7 are met.

4.5 Continuous component quality assurance

4.5.1 General quality assurance requirements

The documented processes shall assure the continuous quality and performance of all components used throughout the production cycle, prior to delivery. This is to assure that the impact of component manufacturer lot to lot variations, lot to lot assembly handling variations, etc., are minimized and controlled. This will assure the delivered components conform to the delivered equipment requirements.

4.5.2 On-going component quality assurance

4.5.2.1 Component manufacturer quality assurance

Components shall be purchased from sources that have been successfully assessed by an accredited component assessment system, which includes a means to assess continuous quality assurance. Such assessment systems include applicable international and industry consensus standards, or the plan owner's approved process for evaluation of the component manufacturer's internal quality assurance processes.

NOTE Examples of government or industry standards are the DOD qualified manufacturers lists, DSCC(JAN), IEC/PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1, AEC-Q100, AEC-Q200, AEC-Q101 and CECC/IECQ approved electronic components suitable for the application.

4.5.2.2 Component quality assurance data

Where the requirement of 4.5.2.1 is not met, the plan owner shall have a process to assure that compliance to the component specification is maintained, either by component manufacturer test or plan owner test.

– A component manufacturer assessment shall include component test processes, ongoing component qualification test plans and acceptance criteria. The method by which this information is obtained shall be documented.

NOTE Typical quality assurance processes include statistical process control, periodic qualification testing, component testing and screening, etc.

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– The plan owner performs quality assurance tests and has documented quality acceptance criteria. Quality assurance tests can also be at either the equipment level or subassembly level.

The following recommendations apply if component level screening is done.

– The components are subjected to screening conditions of sufficient rigor and duration to detect defects.
– A process for screening sampling rates can be proposed by the plan owner, provided that sufficient data is available, and the reject rate is low enough. A process for screening sampling rates may be proposed by the plan owner to reduce from 100 %, provided that sufficient data is available, and the reject rate is low enough.

4.5.3 Plan owner in-house continuous monitoring

The plan owner shall have a process to assure the required performance of components prior to delivery of the equipment. This process includes various levels of processing, assembly and test of the equipment.

A process for identification, recovery and recording of component removals or replacements during in-house processing and testing shall be documented. Significant component replacement trends, equipment repair actions or a pattern of component replacements that are indicative of a potential component problem shall be investigated to determine the root cause. Appropriate corrective actions shall be conducted.

4.5.4 Component design and manufacturing process change monitoring

The process for tracking (or detecting) and monitoring component design and manufacturing process change data shall be documented. The effects of these changes on equipment performance shall be reviewed and assessed. This process could include: direct information from component manufacturers or distributors, sharing technical information sources, other users information, functional or physical analysis during in-house processing. Following analysis, appropriate corrective actions shall be conducted. All design changes shall be in accordance with 4.9.

NOTE 1 Most of the components used in aerospace applications are designed, manufactured and targeted for other industries, and are beyond the control of the plan owner. Frequent design and manufacturing changes are made to improve yield, reduce cost, and enhance performance. Although these changes are documented by the component manufacturer and evaluated for their effects on high-volume applications, their effects on the unique applications of the plan owner may not be evaluated or documented by the component manufacturer. The purpose of this subclause is to describe a process to monitor the components to detect any changes that may affect their performance in the applications of the plan owner.

NOTE 2 Typically, the processes include.

a) Awareness process, such as access to notices of change from the component manufacturer or distributor.
b) An evaluation process, such as periodic functional testing and/or destructive physical analysis or construction analysis (assuming an initial physical analysis) of a sample of each component.
c) Review of the component manufacturer reliability monitor data or quality data to look for failures and other reports of change.

NOTE 3 Alternatively, a process of periodic lot re-qualification of the component can be documented. If used, the periodic lot re-qualification process can be described here and include test frequency, sample size, etc.

4.6 Component availability and associated risk assessment

4.6.1 General

The documented processes shall identify risks associated with availability of the component, and methods to mitigate those risks.

NOTE 1 These can include low volume manufacturers, allocation risks, financial stability of manufacturers, single source manufacturers, etc.

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Components considered to be at risk shall be rated using appropriate metrics that reflect their susceptibility to technology change and obsolescence.

NOTE 2 Input for consideration of metrics can include: technology risk and maturity, life cycle, level of confidence in the manufacturer, predicted obsolescence, monosource component, manufacturer supply file information, imprecise manufacturer specification of component performance (specified as “typical”, not specified, etc.), components other than those readily available in large volumes and identified on avionics technology roadmaps. Use of components outside the manufacturer’s specifications and component obsolescence are specific risk issues that that can be addressed outside of or included in this subclause.

The documented processes shall include tracking and reporting the status of risk mitigation efforts when required by customer or business needs.

The documented processes shall address logistics supportability and life management issues when required by customer or business needs.

The following are primary examples of component risk areas that shall be addressed in the plan, specifically or generically. These risk areas may be addressed as part of other design, production, procurement or marketing processes or practices:

a) new technology availability or maturity for meeting the specified requirements;
b) component delivery and production rate schedules;
c) component obsolescence during design, production, or support;
d) lack of qualification or quality assurance data;
e) qualification test schedule (especially risk of failure);
f) cost drivers (especially with custom components);
g) component changes (design or process changes, known and unknown);
h) quality and reliability of product from a component manufacturer (especially from a new manufacturer);
i) quantification of single event effects rates in components;
j) uprated components;
k) lack of proactive measure for component obsolescence.

NOTE 3 This includes processes used to react to component obsolescence occurrences. They may include bridge stock or life-time buy, identification of alternative sources, equipment re-design, etc.

4.6.2 Component obsolescence

The OEM shall prepare an Obsolescence Management Plan addressing obsolescence issues from design through support including:

- pro-active measures for component obsolescence;
- component obsolescence awareness;
- reaction to component obsolescence.

The plan shall document the processes used by the plan owner to resolve obsolete component occurrences to assure continued production and support as required.

NOTE 1 This includes processes used to react to component obsolescence occurrences. They can include bridge stock or lifetime buys, identification of alternative sources, equipment re-design etc.

IEC/TS 62402 gives guidelines regarding component obsolescence.

4.6.3 Pro-active measures

Pro-active measures for component obsolescence include documented processes that minimize the impact of component obsolescence. These are typically equipment design processes including such activities as inclusion of a component obsolescence forecast,

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disposable electronic modules, or design processes/architectures to accommodate future components.

They may also include a component technology roadmap identifying components with substantial risk of obsolescence.

4.6.4 Component obsolescence awareness

Component obsolescence awareness includes processes that identify existing and impending component discontinuance changes in component design or manufacturing processes. It is recommended that the supplier uses one or more third party obsolescence monitoring applications specific for this purpose.

4.6.5 Reporting

During the contract period of performance, the OEM shall maintain a periodic report of all existing and impending obsolescence issues, even if the obsolescence issue only has impact beyond the contract obligation. This includes cases in which the supplier possesses adequate part inventory to meet contractual delivery obligations, but there is a known issue with future procurement of parts. Additionally, include all instances in which a supplier has announced an End of Life (EOL) or Last Time Buy (LTB) opportunity. This report will be delivered to the customer for review/approval as required in the purchase contract.

The documented processes shall address the issues in 4.6.

4.6.6 Component dependability

The documented processes shall assure the reliability, availability, obsolescence management and maintainability of the components used throughout the customer agreed warranty period or maintenance period and/or agreed lifetime of the equipment provided the end user uses the equipment within the agreed environmental limits.

4.6.7 Semiconductor reliability and wear out

Semiconductor wear out considerations shall be required for high density, highly complex silicon based technology components of design geometries 90 nm and below including SRAM's, SDRAMS, microprocessors, and FPGA's.

Design wear out life of the integrated circuits with feature sizes 90 nm and below should be assessed using available suitable models for the application.

JESD 47 provides guidance for working with component manufacturer to try to determine the wear out life. In the event test data is not available from the manufacturers, or analysis based on up to date models, then the plan owner should demonstrate their own process for achieving satisfactory service life for the application (by analysis, testing, field return survey, etc.). Refer to Annex B for additional information.

4.6.8 Reliability assessment

The documented processes shall verify that the installed component is compatible with the circuit application requirements for performance and reliability through the processes listed in this Technical Specification. These processes include component qualification (including a life test requirement), assurance of quality (consistency), equipment reliability assessments, qualification of the equipment (environmental), and equipment reliability monitors.

When the results of 4.6.7 show that specific parts have a wear out characteristic which is not compatible with the required system operating life, the effect of this wear out and nonlinear failure rate shall be included in the reliability assessment.

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NOTE This can be produced either by using a standard method, component manufacturer reliability tests, equipment field return data, similarity with any other similar applications, etc.

4.7 Component compatibility with the equipment manufacturing process

The documented processes shall assure that the component is compatible with equipment manufacturing processes (without any quality or reliability impact) throughout.

- Component shipping, handling, and storage (short and long term).
- Equipment manufacturing, assembly, shipping, handling, long term storage, test, repair and rework by equipment manufacturer.
- Protection of components from electrostatic discharge (ESD) damage during component storage and handling, during each step of the equipment assembly process. Use of the relevant sections of MIL-HDBK-263, IEC 61340-5-1, and IEC/TR 61340-5-2 will aid in controlling ESD damage.
- Compliance with IEC/PAS 62647-1 (GEIA-STD-0005-1) or IEC/TS 62647-1 that will supersede IEC/PAS 62647-1 and IEC/PAS 62647-2 (GEIA-STD-0005-2) or IEC/TS 62647-2 that will supersede IEC/PAS 62647-2 for the use of lead free terminated components and for lead-free solder assembly if that process is used by the plan owner or his sub-contractors.
- Avoidance of moisture sensitivity damage (MSL) during each step of the equipment assembly process in accordance with IPC/JEDEC J-STD-20.

The documented processes shall identify the key manufacturing, assembly, shipping, handling, storage, test, repair and rework processes by the equipment manufacturer and associated subcontractors; and the plan shall describe how their impact on components is identified, documented and controlled.

The subcontractor shall develop its own ECMP, for all activities subcontracted, and the information shall be accessible to the ECMP assessment team.

4.8 Component data

The plan owner shall have a system for collection, storage, retrieval, analysis and reporting of all relevant data from the component manufacturer, equipment design, equipment manufacturing and equipment use in service; and for keeping the data per customer or regulatory requirements.

The data cannot necessarily reside in one database and may be retrieved from several databases or data retrieval systems across the plan owner's business. A relational approach can be used wherein the data system provides access to the data. For example, if the component qualification data is collected and stored by the component manufacturer, the equipment manufacturer’s data system could consist of a process, software, and hardware to access that data through the component manufacturer’s web page or other source, provided the access is available when needed. As another example, any data that is specific to a program, such as functional simulation results or thermal analysis data, could be accessible via a path through the program data. The plan owner may wish to identify processes that were developed and documented for other initiatives, such as ISO 9000, QS 9000, AS 9000, or IAQS 9100 to satisfy this requirement.

NOTE 1 Typical data includes:

- Component data sheet or specification data, for example, input and output parameters, voltage rating, packaging dimensions, availability data, etc.
- Component application data, for example, functional simulation data, breadboard test data, thermal analysis data, structural analysis data, and electromagnetic emission and susceptibility data.
- Component qualification data, for example, component manufacturer qualification test data, component qualification data collected by the equipment manufacturer, or a third party test house, similarity analysis results, and component in-service data used for qualification.

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- Component quality assurance data, for example, component manufacturer statistical process control data, component manufacturer component screening data, component screening data collected by the equipment manufacturer or a third party test house, and ESS data from higher-level assembly screening used to reduce or eliminate screening.
- Manufacturing and assembly data, for example, equipment manufacturer statistical process control data, ESS data from manufacturing and assembly, and in-process and final functional test.
- Customer reject data.
- In-service data.

NOTE 2 It is anticipated that this information will be available to the customer upon request.

The documented processes shall ensure that the following are available for each component: data sheet, technical and application notes, conditions of use, qualification and quality monitoring data, packaging data, reliability data, availability information, storage conditions, assembly data (for example, soldering conditions) and any additional information to ensure suitability in the application.

Most of the above information can be available from the component manufacturer. If the information is modified, or additional information is required to satisfy this objective, then that information falls within this requirement. Examples include results of additional tests or screens conducted by the plan owner or third parties, programming data, or modifications to the data sheet.

4.9 Configuration control

4.9.1 General

The documented processes shall verify that the equipment configuration control is maintained relative to the component usage in the application. As a minimum requirement, each assembly shall have a controlled parts list. A documented path to the original part manufacturer shall be established. Alternative components shall have an approved process to establish that they are acceptable in the application with the same quality and reliability level.

Each time the documented path is missing, particular qualification or/and additional documentation shall have to be done to ensure compatibility with the application.

NOTE It is anticipated that this information will be available to the customer upon request.

4.9.2 Alternative sources

Alternative sources of components may be qualified and identified in the equipment manufacturer component data base to reduce potential risks to component procurement or to solve an obsolescence or unavailability problem of the previous sources.

In this case, the alternative source component performance (fit, form, function and productibility) shall be fully compliant with the component drawing (or the data sheet and technical performance notes) of the previous component, as described within its selection process.

The alternative source component shall be selected to ensure that the reliability, functionality, performance, interchangeability, etc. of the equipment or assembly is not compromised.

NOTE Attention can be paid to detect “false” alternative sources (the same die or component part type could be packaged, tested and distributed by two or more component manufacturers).

4.9.3 Equipment change documentation

All component substitutions shall be documented. The documentation shall include the following information as per agreement between involved parties (typically between the aircraft manufacturer and avionics equipment manufacturer):

a) CN (change notice) number;

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b) change date;

c) other related CNs;

d) name of the substitute component manufacturer;

e) reason for change;

f) type of customer notification required (see 4.9.4, it is also anticipated that this information will be available to the customer upon request);

g) applications or equipment in which the new component is used;

h) existing component part number;

i) new component part type identification;

j) a statement that the new component is compliant to this plan;

k) impact of the change on reliability, safety, and other critical equipment requirements;

l) required signatures (program manager, component engineer, quality assurance representative, etc.);

m) is the new part uprated? Yes or no.

NOTE Usually, CNs are stored in a controlled, retrievable data system. A copy of the CN form may be included as an annex to the plan.

4.9.4 Customer notifications and approvals

Customer notifications and approvals shall be defined between plan owner and customer, if required. Since the customer notification and approval process is likely to be unique to each customer-supplier relationship, related requirements are beyond the scope of the baseline component management process described in this Technical Specification, and should be documented in the contractual agreements between the supplier and the customer.

4.9.5 Focal organisation

A focal organisation (internal to the plan owner) for configuration control shall be identified in the plan.

5 Plan administration requirements

5.1 Using components outside the manufacturer's specified temperature range

The use of components in their specifications defined and guaranteed by the original component manufacturers is mandatory otherwise it shall be an exception and the requirements listed above shall be addressed.

If components are used outside the temperature ranges specified by the component manufacturer, then the supplier shall demonstrate how he controls this process. In addition to the plan prepared according to this Technical Specification, IEC/TR 62240 also contains recommendations and guidelines on how to do this. Equivalent procedures from other documents may also be acceptable.

A list of these components used outside the temperature range specified by the component manufacturer shall be clearly identified by the plan owner with specific component references and custom drawings. The customer shall be notified with this list upon request.

The use of components outside the temperature ranges specified by the component manufacturer is discouraged.

5.2 Plan organization

The plan shall be organized in such a manner that each of the requirements of Clause 4 is addressed clearly, concisely and unambiguously.

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5.3 Plan terms and definitions

The terms and definitions used in the plan shall be those of Clause 3 of this Technical Specification, unless they are clearly defined otherwise in the plan.

5.4 Plan focal point

The plan shall identify an authority or an organization to serve as the primary interface between the plan owner and outside parties in matters pertaining to the plan.

The plan’s focal point shall:

- assure that the plan is reviewed and updated as necessary,
- ensure that any engineering issues are comprehensively resolved in a timely manner.

NOTE The use of a dedicated functional group, such as a component engineering group, greatly increases the efficiency and effectiveness of implementing and maintaining a plan owner’s ECMP.

5.5 Plan references

The plan shall include a list of references to all the documents referenced in the plan, including this Technical Specification, other industry and government documents, and the plan owner’s internal documents.

5.6 Plan applicability

The plan shall document all the electronic component types or technologies and the range of equipment manufactured by the plan owner to which the plan applies.

NOTE The range of equipment is not intended to be a list of part numbers. It can include, for example, the applicable market segment; for example, “this plan applies to all equipment manufactured for aerospace applications.” It also can include an effectivity date; for example, “this plan applies to all new equipment, and to components substituted into existing equipment.” The range of equipment also can be limited or required by certain contractual agreements.

5.7 Plan implementation

The plan owner shall implement and follow the processes documented in the plan, within its range of applicability. Components selected and managed according to the plan requirements are called ECMP-compliant or plan-compliant components.

5.8 Plan acceptance

The plan shall be accepted when the plan owner and the type certificate holder agree that the plan is acceptable to both parties, if the type certificate holder chooses to exercise the right of plan acceptance. Certification by an assessment body, such as IECQ, may be used as evidence that the plan satisfies the requirements of this Technical Specification.

5.9 Plan maintenance

The plan shall have a 12 month transition time allowed before compliance to the next revision is required.

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Annex A
(informative)

Typical qualification requirements, typical component minimum qualification requirements

This annex is designed to provide guidance on qualification tests for various component types as shown in Table A.1. These tests are suitable for the original equipment manufacturer to demonstrate by testing on a representative sample of components that the component type is suitable for the avionics application.

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Table A.1 – Typical qualification requirements, typical component minimum qualification requirements

Component Type	Typical test method	Suggested minimum qualification requirements	Comments
Hermetic, microcircuits and discrete diodes or transistors	AEC-Q100 IEC PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 EIA/JESD 47 JESD 94 [a] MIL-PRF-38535 MIL-STD-883 or 5962-87517 MIL-PRF-19500	Die – 1) High Operating Life Test (HTOL) 1 000 hours steady state life test at +125 °C, 2) Write/erase endurance life testing for memories 3) Data retention bake for memories , 1 000 hours at +125 °C 4) High Temperature Reverse Bias (HTRB) testing for semiconductors for 1 000 hours at 150 °C 5) Intermittent operating life where applicable for semiconductors for 1 000 hours Hermetic package – 1) Precondition SMT packages 2) Temperature cycling for 100 cycles to MIL-STD-883 method 1010 post electrical testing followed by seal test	Components shall be divided into generic families for testing, see MIL-PRF-38535 for guidelines.
Non hermetic COTS, encapsulated microcircuits and discrete diodes or transistors	AEC-Q100 AEC-Q101 IEC PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 EIA/JESD 47 JESD94[a] MIL-STD-883	Die – 1) High Operating Life Test (HTOL) 1 000 hours steady state life test at +125 °C, sample 2) Write/erase endurance life testing for memories 3) Data retention bake for memories, 1 000 hours at +125 °C 4) High Temperature Reverse Bias (HTRB) testing for semiconductors for 1 000 hours 5) Intermittent operating life where applicable for semiconductors for 1 000 hours Plastic encapsulated package: 1) Precondition SMT packages 2) Temperature cycling for 1000 cycles –55 °C to +125 °C or 500 cycles for –65 °C to +150 °C, 3) Humidity testing: THB 1 000 hours at 85 °C/85 % RH HAST at 130 °C for 96 hours Autoclave 121 °C/100 % RH for 96 hours, 15 psig unbiased THRB for semiconductors followed by electrical testing	Components shall be divided into generic families for testing, see MIL-PRF-38535 or AEC-Q100 or Q101 for guidelines. Samples sizes for the HTOL testing shall be statistically significant to enable calculation of FIT rates for long term Arrhenius high temperature operating life failure rates

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Table A.1 *(continued)*

Component Type	Typical test method	Suggested minimum qualification requirements	Comments
Crystal oscillators	MIL-PRF-55310 AEC-Q200	Crystal – 1) Frequency aging Packaging 2) Vibration 3) Shock 4) For plastic encapsulated: Humidity testing: THB 1 000 hours at 85 °C/85 % RH HAST at 130 °C for 96 hours Autoclave 121 °C/100 % RH for 96 hours, 15 psig unbiased	Components shall be divided into generic families for testing, see MIL-PRF-55310 or AEC-Q100 for guidelines.
Resistors	AEC-Q200 MIL-PRF-55182 MIL-PRF-55342	Resistor element: 1) Load life testing; 1 000 hours or more at max operating temperature Packaging 2) Ceramic un-encapsulated SMT packages: Temperature cycling 3) Plastic encapsulated packages: Moisture resistance or Humidity steady state and temperature cycling	Components shall be divided into generic families for testing, see MIL-PRF-55182 or AEC-Q100 for guidelines. Samples sizes for the load life testing shall be statistically significant to enable calculation of FIT rates for long term Arrhenius high temperature operating life failure rates
Capacitors	AEC-Q200 MIL-PRF-55342	Capacitor element: 1) Load life testing; 1 000 hours or more at max operating temperature Packaging 2) Ceramic un-encapsulated SMT packages: Temperature cycling 3) Plastic encapsulated packages: moisture resistance or humidity steady state and temperature cycling	Components shall be divided into generic families for testing, see MIL-PRF-55 or AEC-Q200 for guidelines. Samples sizes for the load life testing shall be statistically significant to enable calculation of FIT rates for long term Arrhenius high temperature operating life failure rates

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Table A.1 *(continued)*

Component Type	Typical test method	Suggested minimum qualification requirements	Comments
Magnetics	AEC-Q200 MIL-PRF-21028 MIL-PRF-27	Life testing Temperature cycling Humidity Vibration Dielectric Withstand Voltage Insulation resistance	
Connectors	MIL-DTL-38999 series MIL-DTL-5015 MIL-STD-1344 EIA364.09	Life testing Temperature cycling Humidity Durability Vibration Dielectric Withstand Voltage Insulation Resistance	MIL specified external connectors are recommended

[a] JESD94 is used for characterising specific environments.. Therefore review how the component manufacturer has applied JESD 94 for the specific part and analyse each environment to check suitability for the end application.

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Annex B
(informative)

Semiconductor reliability and wear out

Semiconductor wear out considerations may be required for high density, highly complex silicon based technology components of feature size 90 nm and below including SRAM's, SDRAMS, microprocessors, and FPGA's. Devices that have feature sizes above 0,1 µm have been used in avionics applications and in order to perform reliability predictions a constant failure rate with time has been successfully used with no consideration of wear out of the semiconductor device (increasing rate of failure with time). However, by reducing technology feature sizes below 0,1 µm, the internal stresses (power per unit volume, voltage and current) within these devices have greatly increased because the voltage and currents have not reduced as significantly as the geometric feature size reductions. At device feature sizes of about 0,1 µm the increased stresses and resulting degradation mechanisms may impact both the reliability and operating life in the application environment.

Several degradation mechanisms have been investigated and these include hot carrier injection HCI, time dependent dielectric breakdown, TDDB, and negative bias temperature instability, NBTI and electro migration. As a population within equipment during operational usage the devices will degrade away from their initial characteristics and the time at which the devices fail intrinsically in the application is a dependant on a complex function of a large number of factors including feature size, deployment, environmental and application electrical stresses. Investigation of these effects in devices with geometric feature sizes below 0,2 µm has been carried out by the Aerospace Vehicle Systems institute as part of projects AFE17 and 71. Guidance on failure mechanisms and modelling is given in JEP122 and RIAC publication "Physics of Failure Based Handbook of Microelectronics Systems".

Derating the device stressors can mitigate for such mechanisms and may enable the improvement of both the device reliability and the device operating life capability. The derating may take several forms which include voltage derating, operating frequency reduction, part held in standby till required reduction of power dissipated and environment improvement. Methods of thermal derating of semiconductor devices are detailed in JEP149 and methods for determining acceleration factors form testing detailed in JESD91A.

Standards and reference information which can be useful when addressing the wear out requirement are mentioned below:

JESD47F – *JEDEC Solid State Technology Association – Stress-Test-Driven Qualification of integrated Circuits*

JESD91A – *JEDEC Solid State Technology Association – Method for developing acceleration models for electronic failure mechanisms*

JEP122D – *JEDEC Solid State Technology Association – Failure mechanisms and Models for semiconductor devices*

JEP149 – *JEDEC Solid State Technology Association – Application thermal derating methodologies*

Physics-of-Failure Based Handbook of Microelectronic Systems – Available from RiAC (Defense Technology Information Center)

NOTE Contract data services are available to facilitate analysis of component dependability.

Design wear out life of the integrated circuits with feature sizes below 90 nanometers shall be assessed using suitable models for the application.

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Annex C
(informative)

Guidelines for environmental protection techniques, and for comparison of components specifications

Table C.1 shows the environmental protection techniques to be considered during the avionics design process.

Table C.1 – Environmental protection techniques to be considered during the avionics design process

Environmental factor	Component, e.g. microcircuit, diode, transistor, connector etc.	Module or PCB	OEM delivered unit	Aircraft , UAV or satellite bay	Aircraft , UAV, satellite or space unit	Aircraft , UAV, satellite or space unit external
Temperature	Thermal coefficient of expansion trade studies for materials used in modules, MCMs, Hybrids etc. Select lowest thermal resistance package for power components Use largest footprint for power components Heat sinks Peltier cooling Heat pipes Local fan Select components which operate within the manufacturer specified maximum operating and storage temperature ranges Derating Uprate only when no other option available	Match TCE of assembly materials Minimize thermal resistance of power components in assembly PCB heat ladders Plenum cooled Heat planes Heat pipes Heat sink Heaters Thermally micromanaged local component environment to avoid uprating Allow components to self-heat prior to operating to specification limits at cold extremes	Position , e.g. against a cold plate to maximise thermal conduction Provision of forced air Spray cooling Internal cooling Liquid cooling Phase change material (exothermic) cooling Reduce specification requirements	Position electronics in benign environments e.g. within cargo bay or cockpit Keep away from thermal hotspots, e.g. engines, engine hot air vents etc. and cold spots e.g. external areas such as windscreen or tail Supply cooling (Filtered)	Cooling on ground Load sharing Thermal shielding and/or cooling Worldwide geographical use from Artic to Tropical regions	Solar shielding e.g. cockpit and windows of aircraft Solar shielding of satellite

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Environmental factor	Component, e.g. microcircuit, diode, transistor, connector etc.	Module or PCB	OEM delivered unit	Aircraft , UAV or satellite bay	Aircraft , UAV, satellite or space unit	Aircraft , UAV, satellite or space unit external
Humidity	Conformal coating Select plastic encapsulated microcircuits which have passed a HAST humidity test to JESD22-A110 Select components with finishes which will not corrode in humid environments Manage moisture sensitivity of plastic encapsulated SMT components to J-STD-033	Dry PCBs and conformal coat Selection of best conformal coating for humidity environment	Desiccants Hermetic enclosures Dry air Enclosure drainage for rain water or liquid runoff	Dry air supply dehumidifiers Anti-condensation heaters	Dehumidifiers/ desiccants Worldwide geographical use from Artic to Tropical regions	Space external environment is a vacuum but launch sites are typically in tropical areas of the world.

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Environmental factor	Component, e.g. microcircuit, diode, transistor, connector etc.	Module or PCB	OEM delivered unit	Aircraft , UAV or satellite bay	Aircraft , UAV, satellite or space unit	Aircraft , UAV, satellite or space unit external
Vibration	Complaint leading Select physically small components with low mass with lead-frame terminations i.e. minimize LCCs and BGAs Position away from vibration nodes RTV Lacing Local potting Select vibration ruggedized components for very high vibration levels: 1) Use hard gold plated connector contacts to prevent 'fretting' 2) Use high vibration crystals and oscillators 3) Use semiconductor timing microcircuits instead of crystals if operating temperature permits 4) Select high vibration circuit breakers, relays and contactors. 5) Vibration test large components e.g. displays, power suppliers, as part of component qualification testing to minimize unit qualification risk	Stiffeners (reduce flexing) of PCB Local anti-vibration mounting Potting or RTV Lacing of cables or wires Keep length of cables and interconnect relatively short, evaluate cable chaffing, ensure sufficient strain relief in cables. Use strain-relief connector back-shells to protect wires.	Anti- vibration mounts Position (benign) Vibration analysis of nodes and redesign as required to minimize PWB deflections and stress on components.	Position Active cancellation Anti-vibration mounts Position (benign) – keep electronics away from engines, gun fire positions, doors, wheel-wells etc.	Determined by aircraft operation i.e. military, civil or space Military aircraft may have several additional vibration requirements e.g. gunfire, acoustic noise, etc.	Design

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Environmental factor	Component, e.g. microcircuit, diode, transistor, connector etc.	Module or PCB	OEM delivered unit	Aircraft , UAV or satellite bay	Aircraft , UAV, satellite or space unit	Aircraft , UAV, satellite or space unit external
EMI/EMC	Local shield Local supply filtering/ regulation Review COTS Transient suppressor (TVS) requirements	System architecture – Circuit function partitioning Local shielding Local module Supply/filtering Improved grounding – check ground loops	Position Additional shielding Reduced electrical connectivity	Reduced electrical connectivity Shielded bay Maximize optical signalling	Maximize optical signalling	Composite structures may increase EMC requirements
Altitude	Void free component encapsulation e.g. transformers, encapsulated modules	Void free PCBs and conformal coatings. Review minimum spacings / gaps to avoid flashover during DWV and IR testing at altitude	Hermetic enclosure / pressurized enclosure / venting valves	Pressurized bay	Determined by aircraft operational profile i.e. military, civil or space	
Shock/ acceleration	As vibration					
Power supply	Local supply filtering	Local module power supply	Local conditioning		Load sharing/filtering	
Long term dormant storage	Select plastic encapsulated components which have passed a HAST humidity test to JESD22-A110 Store under dry nitrogen Store wafers under dry nitrogen instead of assembled components	Conformal coat Desiccants Dry bag/desiccants Store in dry nitrogen cabinets	Desiccants Hermetic enclosures Dry air storage for long term storage of units	Dry atmospheric storage	Dry atmospheric storage	

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Environmental factor	Component, e.g. microcircuit, diode, transistor, connector etc.	Module or PCB	OEM delivered unit	Aircraft , UAV or satellite bay	Aircraft , UAV, satellite or space unit	Aircraft , UAV, satellite or space unit external
Atmospheric SEU radiation	Select components, e.g. memories not subject to SEU effects Select components, e.g. memories not subject to SEL Test components of a certain die revision or lot date code for atmospheric SEU susceptibility to IEC/TS 62396-2 and consider One Time Buys Select components which do not use Boron 10 Derate SEU susceptible high voltage components	System architecture design mitigation techniques to IEC TS 62396-3 Design PCB assemblies with no single point failures	System architecture design mitigation techniques to IEC/TS 62396-3	Select location and materials to minimize thermal neutron magnification effects Select components which do not use Boron materials	Maximum attitude of operation, as the effects are harder to manage the higher the altitude is.	
Total dose radiation effects for space use	Select components immune to total dose radiation effects Select components, e.g. memories not subject to SEL or SEU Test components of a certain die revision or lot date code and carry out One Time Buys	System architecture design mitigation techniques Design PCB assemblies with no single point failures	System architecture design mitigation			
Semiconductor wear out	Derate Select older design geometry (> 90 nm) components which are less susceptible to these effects	Design PCB assemblies with no single point failures Use dual redundancy circuit techniques to minimize effects Design PCB upgrades for maintainability programs	Maintainability plans for components susceptible to early wear out			

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Table C.2 gives guidelines for the comparison of internationally available component specifications – Microcircuits.

Table C.2 – Guidelines for the comparison of internationally available component specifications – Microcircuits[a]

Environmental or audit test conditions	Consideration with document: STACK S/0001 revision 14 or IEC/PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 – typically COTS, packaging is plastic encapsulated but can be hermetic	Consideration with document: JESD47G – typically COTS, packaging is plastic encapsulated but can be hermetic[b]	Consideration with document: JESD94 typically COTS, packaging is typically plastic encapsulated[b]	Consideration with document: AEC-Q100, Rev G, automotive,[b] typically COTS plastic encapsulated	Consideration with document: AQEC IEC/TS 62564-1: 2012 typically COTS 'Enhanced' Plastic encapsulated	Consideration with document: 5962-87517 typically hermetically packaged to MIL-STD-883	Consideration with document: MIL-PRF-38534 typically hermetically packaged using MIL-STD-883 method 5004 and method 5005
Are all requirements third party audited?	Yes, by STACK as part of 'STACK Certification' program where any reduced testing for marketing reasons is defined as 'Limitations'. This is a generic quality process audit with random product audits. Possible IECQ audits in the near future	No – JEDEC has no audit function	JEDEC has no audit function. JESD94 can be used with JESD47 where testing is customised for known failure mechanisms, e.g. temperature cycling, humidity, life testing	Yes. A TS 16949 third party quality systems audit is required in addition to the components passing all AEC-Q100 tests which are reviewed and approved by the automotive user	The basic part selected may be third party audited if it is from a STACK Certified manufacturer or is an AEC-Q100 approved component. The additional AQEC data is difficult to audit as the data set will be different for each component.	Yes	Yes and test results are approved by DLA
Is the scheme a standard 'stress test' style qualification method?	Yes	Yes	No. Testing is customised for the end application for known failure mechanisms where the test duration and conditions vary on application variables. Does not cover characterisation tests or 'go/no-go' type tests.	Yes	Yes plus additional AQEC test data	Yes	Yes

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Environmental or audit test conditions	Consideration with document: STACK S/0001 revision 14 or IEC/PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 – typically COTS, packaging is plastic encapsulated but can be hermetic	Consideration with document: JESD47G – typically COTS, packaging is plastic encapsulated but can be hermetic[b]	Consideration with document: JESD94 typically COTS, packaging is typically plastic encapsulated[b]	Consideration with document: AEC-Q100, Rev G, automotive,[b] typically COTS plastic encapsulated	Consideration with document: AQEC IEC/TS 62564-1: 2012 typically COTS 'Enhanced' Plastic encapsulated	Consideration with document: 5962-87517 typically hermetically packaged to MIL-STD-883	Consideration with document: MIL-PRF-38534 typically hermetically packaged using MIL-STD-883 method 5004 and method 5005
Is this a customised qualification program where JESD47 or similar stress testing is inappropriate?	No	No	Yes for known failure mechanisms where the test duration and conditions vary on application variables.	No	No	No	No
Oxide integrity of wafer	Yes – JP001.01	Yes – JP001.01	Customised for application	Yes	Typically included to JP001.01	Yes as part of wafer acceptance criteria per Appendix H	Yes as part of wafer acceptance criteria per Appendix H
Electromigration of wafer	Yes – JEP119 or JP001.01	Yes – JEP119	Customised for application	Yes	Typically included to JP001.01	Yes as part of wafer acceptance criteria per Appendix H	Yes as part of wafer acceptance criteria per Appendix H
Hot carrier injection testing on wafer	Yes – JEP001.01	Yes – JP001.01	Customised for application	Yes	Typically included to JP001.01	Yes as part of wafer acceptance criteria per Appendix H	Yes as part of wafer acceptance criteria per Appendix H
Negative bias instability testing on wafer	To be added at next revision	Yes – JP001.01	Customised for application	Yes	Typically included to JP001.01	Considered part of wafer acceptance	Considered part of wafer acceptance
Time dependant dielectric breakdown	Yes – JEP001.01	Yes – JP001.01	Customised for application	Yes	Typically included to JP001.01	Yes as part of wafer acceptance criteria per Appendix H	Yes as part of wafer acceptance criteria per Appendix H

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Environmental or audit test conditions	Consideration with document: STACK S/0001 revision 14 or IEC/PAS 62686-1 or IEC/TS 62686-1 that will supersede IEC/PAS 62686-1 – typically COTS, packaging is plastic encapsulated but can be hermetic	Consideration with document: JESD47G – typically COTS, packaging is plastic encapsulated but can be hermetic[b]	Consideration with document: JESD94 typically COTS, packaging is typically plastic encapsulated[b]	Consideration with document: AEC-Q100, Rev G, automotive,[b] typically COTS plastic encapsulated	Consideration with document: AQEC IEC/TS 62564-1: 2012 typically COTS 'Enhanced' Plastic encapsulated	Consideration with document: 5962-87517 typically hermetically packaged to MIL-STD-883	Consideration with document: MIL-PRF-38534 typically hermetically packaged using MIL-STD-883 method 5004 and method 5005
Stress migration	Yes – JEP001.01	Yes – JP001.01	Customised for application	Yes	Typically included	Yes as part of wafer acceptance criteria per Appendix H	Yes as part of wafer acceptance criteria per Appendix H
Internal visual	Yes – MIL-STD883 method 2010	Not mentioned	No	Not mentioned	Yes if requested	Yes – MIL-STD883 method 2010	Yes – MIL-STD883 method 2010
Material restrictions	Allows RoHS compliant components, including tin termination finishes	Allows RoHS compliant components, including tin termination finishes	No	Allows RoHS compliant components, including tin termination finishes	Typically allows RoHS compliance but can be tailored for tin/lead if requested	Yes – Not RoHS compliant, tin platings not allowed, some internal material restrictions	Yes – Not RoHS compliant, tin platings not allowed, some internal material restrictions
Electrical testing over –55 °C to +125 °C range	Yes for hermetic components. No for plastic encapsulated components. Some are tested: –40 °C to +125 °C or –40 °C to +105 °C or –40 °C to +85 °C	Yes for hermetic components. No for plastic encapsulated components. Some are tested: –40 °C to +125 °C or –40 °C to +105 °C or –40 °C to +85 °C	No	No but either: –40 °C to +125 °C or –40 °C to +105 °C or –40 °C to +85 °C	Yes if this temperature range is requested. Other options include: –40 °C to +125 °C or –40 °C to +105 °C or –40 °C to +85 °C	Yes	Yes

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