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Integrated circuits – EMC evaluation of transceivers – Part 5: Ethernet transceivers

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INTEGRATED CIRCUITS – EMC EVALUATION OF TRANSCEIVERS –

Part 5: Ethernet transceivers

FOREWORD

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International Standard IEC 62228-5 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47A/1115/FDIS	47A/1117/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
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INTEGRATED CIRCUITS – EMC EVALUATION OF TRANSCEIVERS –

Part 5: Ethernet transceivers

1 Scope

This part of IEC 62228 specifies test and measurement methods for EMC evaluation of Ethernet transceiver ICs under network condition. It defines test configurations, test conditions, test signals, failure criteria, test procedures, test setups and test boards. It is applicable for transceiver of the Ethernet systems

- 100BASE-T1 according to ISO/IEC/IEEE 8802-3/AMD1;
- 100BASE-TX according to ISO/IEC/IEEE 8802-3;
- 1000BASE-T1 according to ISO/IEC/IEEE 8802-3/AMD4

and covers

- the emission of RF disturbances;
- the immunity against RF disturbances;
- the immunity against impulses;
- the immunity against electrostatic discharges (ESD).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-1, *Integrated circuits – Measurement of electromagnetic emissions – Part 1: General conditions and definitions*

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method*

IEC 62132-1, *Integrated circuits – Measurement of electromagnetic immunity – Part 1: General conditions and definitions*

IEC 62132-4, *Integrated circuits – Measurement of electromagnetic immunity 150 kHz to 1 GHz – Part 4: Direct RF power injection method*

IEC 62215-3, *Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method*

IEC 62228-1, *Integrated circuits – EMC evaluation of transceivers – Part 1: General conditions and definitions*

ISO 10605, *Road vehicles – Test methods for electrical disturbances from electrostatic discharge*

ISO 21111-2, *Road vehicles – In-vehicle Ethernet – Part 2: Common physical entity requirements*

ISO 7637-2, *Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*

ISO/IEC/IEEE 8802-3:2017, *Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Standard for Ethernet*

ISO/IEC/IEEE 8802-3:2017/AMD1:2017, *Amendment 1 – Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Standard for Ethernet – Physical layer specifications and management parameters for 100 Mb/s operation over a single balanced twisted pair cable (100BASE-T1)*

ISO/IEC/IEEE 8802-3:2017/AMD4:2017, *Amendment 4 – Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements – Part 3: Standard for Ethernet – Physical layer specifications and management parameters for 1 Gb/s operation over a single twisted-pair copper cable*

Electronic Components Industry Association, EIA-198-1, *Ceramic Dielectric Capacitors Classes I, II, III and IV*

3 Terms, definitions and abbreviated terms

For the purposes of this document, the terms and definitions given in IEC 61967-1, IEC 62132-1, IEC 62228-1, as well as the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at http://www.iso.org/obp
- IEC Electropedia: available at http://www.electropedia.org/

3.1 Terms and definitions

3.1.1
100BASE-T1 transceiver
transceiver 100 Mbit/s via single balanced twisted pair, with a functionality according to ISO/IEC/IEEE 8802-3/AMD1 (100BASE-T1)

3.1.2
100BASE-TX transceiver
transceiver 100 Mbit/s via two balanced twisted pairs, with a functionality according to ISO/IEC/IEEE 8802-3(100BASE-TX)

3.1.3
1000BASE-T1 transceiver
transceiver 1000 Mbit/s via single balanced twisted pair, with a functionality according to ISO/IEC/IEEE 8802-3/AMD4 (1000BASE-T1)

3.1.4
global pin
pin that carries a signal or power, which enters or leaves the application board without any active component in between

3.1.5
local pin
pin that carries a signal or power, which does not leave the application board

3.1.6
mandatory components
pl
components needed for proper function and/or technical requirement of IC as specified by the IC manufacturer

3.1.7
switch
IC with integrated Ethernet transceivers and switch functionality as defined in ISO/IEC/IEEE 8802-3

3.2 Abbreviated terms

ASIC	Application specific integrated circuit
BIN	Bus interface network
BIST	Built in self-test
CMC	Common mode choke
CDMR	Common to differential mode conversion ratio
CMR	Common mode rejection
DCMR	Differential to common mode conversion ratio
DPI	Direct RF power injection
DTT	Data transfer test
DUT	Device under test
FPGA	Field programmable gate array
GMII	Gigabit media independent interface
GPIO	General purpose input or output
IL	Insertion loss
INH	Inhibit
LCL	Longitudinal conversion loss
LPF	Low pass filter
MDI	Medium dependent interface
MII	Media independent interface
PCB	Printed circuit board
PRBS	Pseudo random bit stream
PHY	Ethernet single transceiver
RGMII	Reduced gigabit media independent interface
RL	Return loss
RS-FEC	Reed Solomon forward error correction
SBC	System base chip
SGMII	Serial gigabit media independent interface
SNR	Signal-to-noise ratio
S-parameter	Scattering parameter
SQI	Signal quality indicator
TDR	Time domain reflectometry

TLP	Transmission line pulse
VNA	Vector network analyzer

4 General

The intention of this document is to evaluate the EMC performance of Ethernet transceivers under application conditions in a minimal network.

The evaluation of the EMC characteristics of Ethernet transceivers shall be performed for the implemented functional operation modes as defined in Table 1 under network condition for conducted RF emission and RF immunity tests and impulse immunity tests and on a single transceiver IC for electrostatic discharge tests.

The aim of these tests is to determine the EMC performance on dedicated pins of the Ethernet transceiver which are considered as EMC relevant in the application. For an Ethernet transceiver, these pins are global pins like MDIP, MDIN, V_{BAT} and WAKE as well as local pins like power supply inputs (V_{DDx}). The global pin WAKE is given as an example and represents any global pin other than MDI and voltage supply V_{BAT}.

If the DUT includes additional product specific EMC relevant pins (functions), it shall be tested as well. The test conditions and failure validation criteria shall be adapted to the definitions for the standard functionality of Ethernet transceivers.

The test methods used for the EMC characterization are based on the international standards for IC EMC tests and are described in Table 1.

Table 1 – Overview of measurements and tests

Configuration	Test	Test method	Evaluation	Functional operation mode
Transceiver network	RF conducted emission (EMI)	150 Ω direct coupling (IEC 61967-4)	Spectrum	Normal
	RF conducted immunity (RF)	DPI (IEC 62132-4)	Function	Normal
				Low power
	Impulse immunity (IMP)	Non-synchronous transient injection (IEC 62215-3)	Function	Normal
				Low power
	ESD powered	Contact discharge (ISO 10605)	Function	Normal
				Low power
Single transceiver	ESD unpowered	Contact discharge (ISO 10605)	Damage	Unpowered

The 150 Ω direct coupling, DPI and impulse immunity test methods are chosen for the evaluation of the conducted EMC characteristic of transceivers in network condition. These three test methods are based on the same approach using conductive coupling. Therefore, it is possible to use the same test board for all tests in functional operation mode, which reduces the effort and increases the reproducibility and comparability of test results.

Powered ESD test will be performed using the same approach of testing the Ethernet transceiver under network conditions but a modified test board is used because of RF and ESD tests cannot be combined on one test board if all specific test conditions of each test method should be covered.

The unpowered ESD test is performed on a separate test board with a single transceiver.

All measurements and tests should be done according to the general drawings of schematics given in Annex A with soldered transceivers on special test boards as described in Annex B to ensure application like conditions and avoid setup effects by sockets. Recommended limits for Ethernet transceivers in automotive application are given in Annex D.

In general, the test definition is done for Ethernet single transceiver (PHY). Ethernet transceiver cells embedded in switches, SBCs or ASICs shall follow the test methods for PHYs, adapting test conditions and targets as necessary. Such adaptations shall be done individually for the dedicated IC but shall follow the general definitions.

If an Ethernet transceiver supports more than one Ethernet system (e.g. 100BASE-T1 and 1000BASE-T1), all tests for the implemented Ethernet systems shall be performed separately.

In order to verify filter effects on the EMC performance of Ethernet transceivers, configurations with different bus interface networks for MDI are defined in this document. In consequence the frequency characteristic of these filter elements shall be taken into account for the interpretation of the test results.

5 Test and operating conditions

5.1 Supply and ambient conditions

For all tests and measurements under operating conditions, the settings are based on systems with 12 V power supply, which is the main application of Ethernet transceivers. If a transceiver is designed or targeted for other power supply voltages, the test conditions and test targets shall be adapted and documented accordingly. The defined supply and ambient conditions for functional operation are given in Table 2.

Table 2 – Supply and ambient conditions for functional operation

Parameter	Value
Voltage supply V_{BAText}	(14 ± 0,2) V (default)
Voltage supply V_{DDx}	$V_{nominal}$ ± 2 %
Test temperature	(23 ± 5) °C

For RF emission measurements, the ambient noise floor shall be at least 6 dB below the applied target limit and documented in the test report.

For ESD tests, the requirements of ISO 10605 climatic environmental conditions shall be applied.

5.2 Test operation modes

5.2.1 General

The Ethernet transceiver shall be tested in functional operation modes and unpowered mode according to Table 1.

Depending on the transceiver the configuration for functional operation modes is controlled by hardware and/or software settings.

5.2.2 Transceiver configuration for normal operation mode

For test in normal functional operation mode, a transceiver configuration according to Table 3 shall be used.

Table 3 – Definition for transceiver configuration for normal operation mode

Topic	Content
Transceiver configuration	– full duplex mode with maximum data rate for DUT – automatic polarity detection enabled – transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report)

5.2.3 Transceiver configuration for low power mode

For test in low power mode a transceiver configuration according to Table 4 shall be used.

Table 4 – Definition for transceiver mode configuration for low power mode

Topic	Content
Transceiver configuration	– transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report)

5.3 Definition of BIN

For test of 100BASE-T1 and 1000BASE-T1 transceivers, the following MDI test networks (BIN) are defined:

- Minimum MDI interface network (Min-BIN):
  DC blocking capacitor $C_{ac1} = C_{ac2}$ = 100 nF as illustrated in Figure 1.
- Standard MDI interface (Std-BIN):
  DC blocking capacitor $C_{ac1} = C_{ac2}$ = 100 nF and a CMC that meet the recommendations of Annex E as illustrated in Figure 2.
- Optimized MDI interface (Opt-BIN):
  DC blocking capacitor $C_{ac1} = C_{ac2}$ = 100 nF and a CMC that meet the recommendations of Annex E, a Low pass filter (LPF) and a ESD suppression devices or terminations defined by semiconductor manufacturer as illustrated in Figure 3. The position of ESD suppression devices within the interface network can either be between transceiver and CMC and / or between C_{ac1} and C_{ac2} and MDI node.

NOTE 1 Min-BIN and Std-BIN are defined to provide data for comparison of the EMC characteristics of different Ethernet transceivers. Opt-BIN is intended to use for evaluation of EMC characteristics of the tested Ethernet transceivers.

NOTE 2 For DC blocking capacitors C_{ac1} and C_{ac2}, the capacitance C = 100 nF is set as default value for tests. Other capacitor values, defined by semiconductor manufacturer, are also possible to use.

NOTE 3 As an alternative to the DC blocking capacitors C_{ac1} and C_{ac2} in combination with a CMC, a magnetics according to ISO/IEC/IEEE 8802-3, defined by semiconductor manufacturer, is also possible to use.

NOTE 4 The characteristics of ESD suppression device can be evaluated according to the definitions of Annex F.

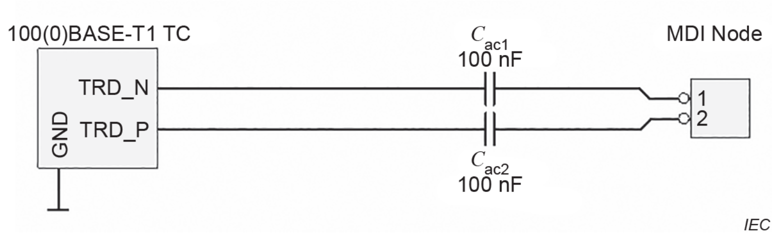


Figure 1 – Minimum MDI interface test network (Min-BIN)

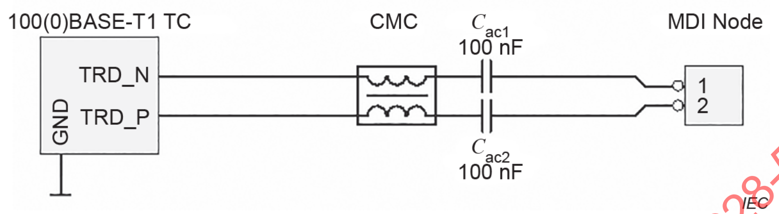


Figure 2 – Standard MDI interface test network (Std-BIN)

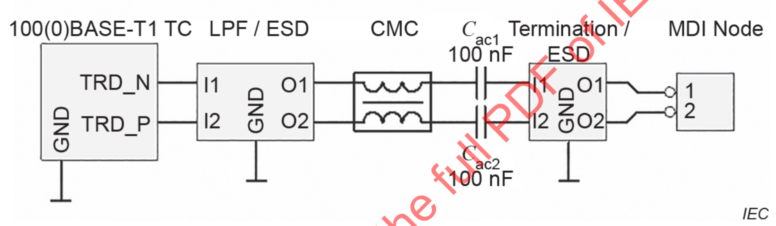


Figure 3 – Optimized MDI interface test network (Opt-BIN)

The S-parameter S_{CC21}, S_{DD21}, S_{DC21} and S_{CD21} of CMC samples used for testing may be measured or prepared by the manufacturer according to Annex E and shall be documented in the test report.

For test of 100BASE-TX transceivers, there is only an optimized MDI interface (Opt-BIN) defined. The Opt-BIN network as defined by the semiconductor manufacturer shall be used.

5.4 Test configuration

5.4.1 General configuration for transceiver network

For evaluation of conducted RF emission and RF immunity as well as impulse immunity characteristic of an Ethernet transceiver in functional operation mode, a minimal Ethernet test network consisting of two Ethernet transceivers of same type shall be used.

The test configuration in general consists of Ethernet transceivers with external mandatory components (Ethernet node) in a minimal test network, where filtered power supplies, signals, monitoring probes and coupling networks are connected as shown in Figure 4. The definitions for BIN are given in 5.3.

Both nodes are configured according to the data sheet of the semiconductor manufacturer to establish a full duplex Ethernet link. This connection is carried out as line impedance controlled PCB traces and not a wire connection.

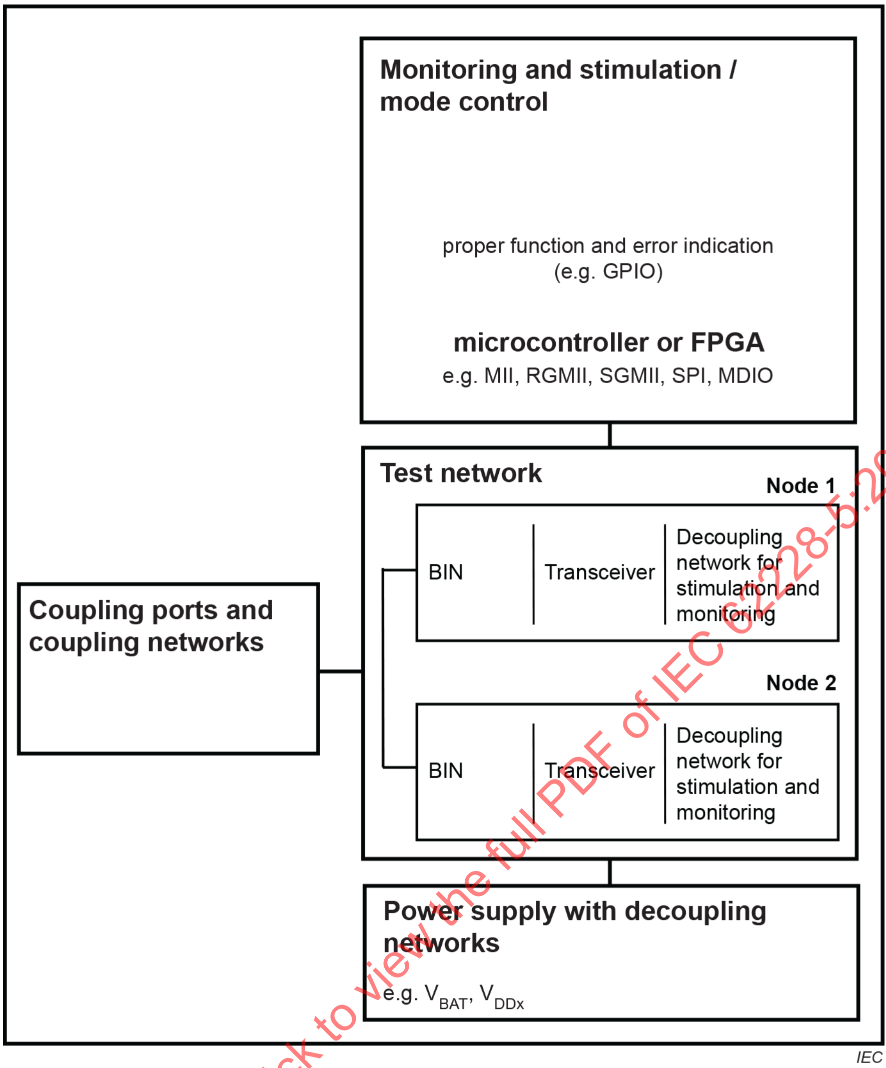


Figure 4 – General test configuration for tests in transceiver network for conducted tests

NOTE 1 In specific cases or for analyses a deviation from this setup can be agreed between the users of this document and will be noted in the test report.

The microcontroller or FPGA is used for configuring and monitoring the Ethernet transceiver and for generating a test communication. For this purpose, it should be able to operate with the communication interfaces that are supported by the tested Ethernet transceiver (e.g. MII, RGMII and SGMII).

If Ethernet transceivers support multiple MII interfaces in minimum two of them should be used for the configuration of the transceiver network. The selection recommendation is given in Table 5.

NOTE 2 Other MII interfaces e.g. RMII and GMII can be used for testing in addition but this is not required.

Table 5 – Selection recommendation of MII interfaces for transceiver network configuration

Ethernet system	MII interface type 1	MII interface type 2
100BASE-T1	MII	RGMII
100BASE-TX	MII	RGMII
1000BASE-T1	RGMII	SGMII

Node 1 should be configured with MII interface type 1 and node 2 with MII interface type 2. If only one interface type is implemented, both nodes are configured with the same available interface (MII or RGMII or SGMII).

In most cases, it is beneficial to use a microcontroller or FPGA per Ethernet node. The microcontroller or FPGA shall be EMC decoupled from the tested transceiver (and its EMC coupling networks) using filter networks at voltage supplies. Specific layout requirements shall be considered. A specific software implementation runs on the microcontroller or FPGA which should be adapted to the transceiver type, especially for configuration and monitoring.

If a switch or an IC with more than one integrated Ethernet transceiver (e.g. Dual PHY) shall be evaluated, each port that is intended to be used for wired Ethernet communication shall be tested separately. For that purpose, the tested port of node 1 shall be connected with the same port of node 2 (port 1 to port 1, port 2 to port 2, etc.).

General drawings of schematics with more details are given in Annex A.

5.4.2 General configuration for single transceiver

The general test configuration for unpowered ESD test of Ethernet transceivers consists of a single Ethernet transceiver with external mandatory components on a test board with discharge coupling networks as shown in Figure 5.

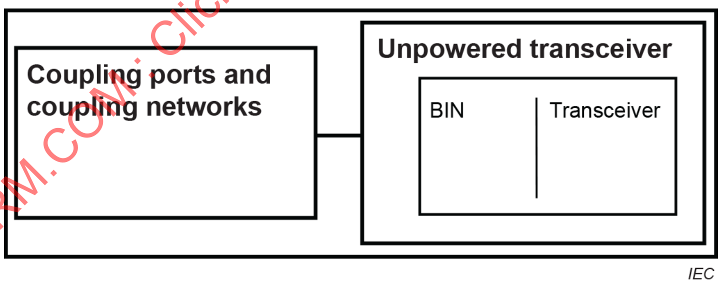
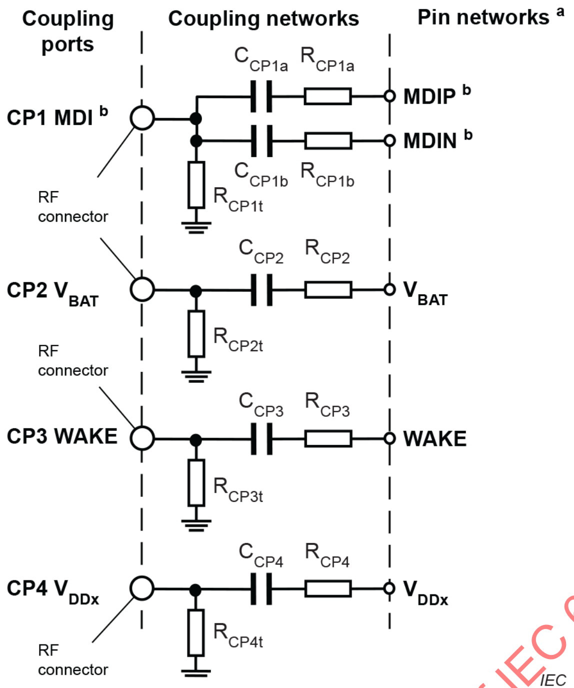


Figure 5 – General test configuration for unpowered ESD test

5.4.3 Transceiver network tests – coupling ports and networks for conducted tests

The coupling ports and coupling networks are used to transfer disturbances to or from the test network with a defined transfer characteristic. The schematic of the coupling ports, networks and pins are shown in Figure 6. The values of the components are dependent on the test method and defined in Table 6. The tolerance of the components shall be 1 % or less. For the resistors R_{CP1a} and R_{CP1b} used for symmetrical coupling, a maximum mismatch of 0,1 % is recommended.

NOTE Components can be selected by measurement of their value.



[a] The pin networks include all external mandatory components for the respective pin or pins.

[b] The pins MDIP and MDIN represent all pins of the transceiver that are connected to the MDI of 100BASE-T1 and 1000BASE-T1 transceivers. For 100BASE-TX transceivers a second MDI coupling network is required for testing the second path of the Ethernet link.

Figure 6 – Transceiver network tests – coupling ports and networks

Table 6 – Transceiver network tests – component value definitions of coupling ports and networks

Port	Type	Purpose	Component		
			$R_{CP1..4}$	$C_{CP1..4}$	$R_{CP1..4t}$
CP1	EMI1	RF symmetrical emission measurement on MDI	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	EMI1a	RF asymmetric emission measurement on MDI (+ 1,25 %)	R_{CP1a} = 121 Ω R_{CP1b} = 119,5 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	EMI1b	RF asymmetric emission measurement on MDI (- 1,25 %)	R_{CP1a} = 119,5 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	EMI1c	RF asymmetric emission measurement on MDI (+ 2,5 %)	R_{CP1a} = 121 Ω R_{CP1b} = 118 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	EMI1d	RF asymmetric emission measurement on MDI (- 2,5 %)	R_{CP1a} = 118 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	EMI1e	RF asymmetric emission measurement on MDI (+ 5 %)	R_{CP1a} = 121 Ω R_{CP1b} = 115 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	EMI1f	RF asymmetric emission measurement on MDI (- 5 %)	R_{CP1a} = 115 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	R_{CP1t} = 51 Ω
	RF1	RF symmetrical coupling for immunity test on MDI	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	RF1a	RF asymmetrical coupling for immunity test on MDI (+ 1,25 %)	R_{CP1a} = 121 Ω R_{CP1b} = 119,5 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	RF1b	RF asymmetrical coupling for immunity test on MDI (- 1,25 %)	R_{CP1a} = 119,5 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	RF1c	RF asymmetrical coupling for immunity test on MDI (+ 2,5 %)	R_{CP1a} = 121 Ω R_{CP1b} = 118 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	RF1d	RF asymmetrical coupling for immunity test on MDI (- 2,5 %)	R_{CP1a} = 118 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	RF1e	RF asymmetrical coupling for immunity test on MDI (+ 5 %)	R_{CP1a} = 121 Ω R_{CP1b} = 115 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	RF1f	RF asymmetrical coupling for immunity test on MDI (- 5 %)	R_{CP1a} = 115 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	IMP1	Impulse coupling on MDI	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 470 pF C_{CP1b} = 470 pF	not used
	ESD1 IND	Indirect ESD coupling on MDIP, MDIN [a]	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 33 pF C_{CP1b} = 33 pF	R_{CP1t} = 220 kΩ [b]
CP2	EMI2	RF emission measurement on V_{BAT}	R_{CP2} = 120 Ω	C_{CP2} = 6,8 nF	R_{CP2t} = 51 Ω
	RF2	RF coupling for immunity test on V_{BAT}	R_{CP2} = 0 Ω	C_{CP2} = 6,8 nF	not used
	IMP2	Impulse coupling on V_{BAT}	R_{CP2} = 0 Ω	Shorted	not used
CP3	EMI3	RF emission measurement on WAKE	R_{CP3} = 120 Ω	C_{CP3} = 6,8 nF	R_{CP3t} = 51 Ω
	RF3	RF coupling for immunity test on WAKE	R_{CP3} = 0 Ω	C_{CP3} = 6,8 nF	not used
	IMP3	Impulse coupling on WAKE	R_{CP3} = 0 Ω	C_{CP3} = 1,0 nF	not used

Port	Type	Purpose	Component		
			$R_{CP1..4}$	$C_{CP1..4}$	$R_{CP1..4t}$
CP4	EMI4	RF emission measurement on V_{DDX}	R_{CP4} = 120 Ω	C_{CP4} = 6,8 nF	R_{CP4t} = 51 Ω

The parasitic inductance value of all resistors and capacitors used for RF emission and immunity coupling networks shall be less than 2 nH.

R_{CP1a} and R_{CP1b} can be combined out of two resistors of the same type.

[a] All used resistors of the ESD coupling network shall be specified as ESD-robust up to the maximum used discharge voltage level. The specified peak voltage of used capacitors shall be at least 3 kV. The value for the coupling capacitance is estimated related to the test setup for indirect ESD test defined in ISO 10605.

[b] The resistor R_{CP1t} is used optional to avoid static pre-charge of discharge point caused by the ESD generator. A spark over at these resistors at high test levels shall be avoided. If a static pre-charge is prevented by the ESD generator construction, these resistors are not needed. Alternatively, an external resistor can be used to remove pre-charges of each discharge point before each single test.

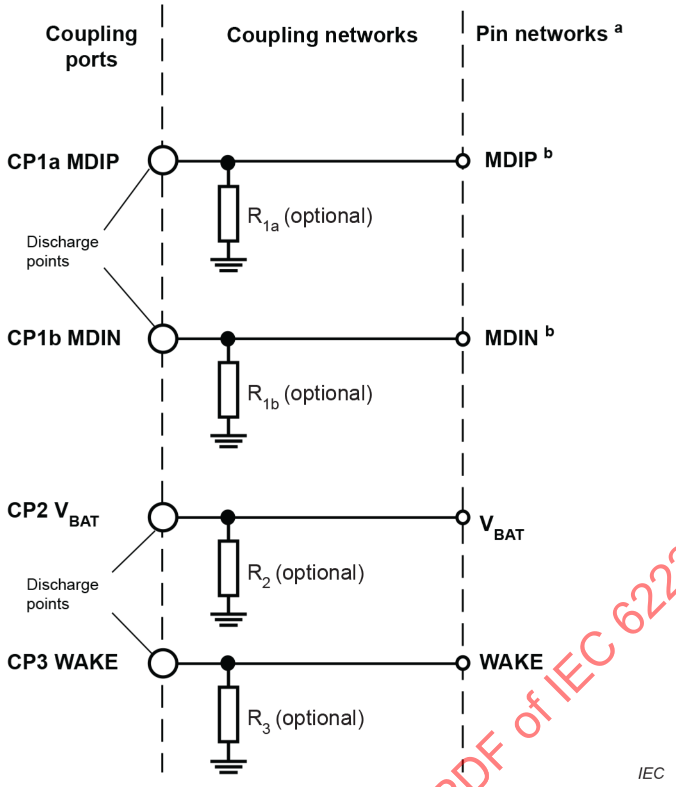
The test configurations with coupling ports and coupling networks connected to the Ethernet test network are given in the general drawing of schematics in Figure A.1.

The characterization of the coupling ports and coupling networks is carried out as follows:

The magnitude of insertion losses (S_{21} measurement) between the ports (CP1 to CP4) and the inputs of the respective transceiver pin network on the test board shall be measured and documented in the test report. The connection of signal pads using 50 Ω coaxial probe directly and ground connection shall be as short as possible. For this characterization the coupling port shall be configured for RF immunity or emission test and the Ethernet transceivers with all components of the MDI test network (BIN) shall be removed. All other components which are directly connected to the coupling port (e.g. filter to power supply or loads) remain on the test board.

5.4.4 Single transceiver tests – coupling ports and networks

The discharge points are connected by the coupling networks to the Ethernet transceiver test circuitry. The schematic and definitions of the coupling ports, networks and pins used for unpowered ESD tests are given in Figure 7 and Table 7.



[a] The pin networks include all external mandatory components and for the respective pin or pins.

[b] The pins MDIP and MDIN represent all pins of the transceiver that are connected to the MDI of 100BASE-T1 and 1000BASE-T1 transceivers. For 100BASE-TX transceivers a second MDI coupling network is required for testing the second path of the Ethernet link.

Figure 7 – Coupling ports and networks for unpowered ESD tests

Table 7 – Definitions of coupling ports for unpowered ESD tests

Port	Type	Purpose	Components
CP1a	ESD1a	Direct ESD coupling on MDIP	metal trace for galvanic connection [a]
CP1b	ESD1b	Direct ESD coupling on MDIN	metal trace for galvanic connection [a]
CP2	ESD2	Direct ESD coupling on V_{BAT}	metal trace for galvanic connection [a]
CP3	ESD3	Direct ESD coupling on WAKE	metal trace for galvanic connection [a]

[a] The optional resistors R_{1a}, R_{1b}, R_2 and R_3 with $R \leq 220$ kΩ are used to avoid static pre-charge of discharge point caused by the ESD generator. A spark over at these resistors at high test levels shall be avoided. If a static pre-charge is prevented by the ESD generator construction, these resistors are not needed. Alternatively, an external resistor can be used to remove pre-charges of each discharge point before each single test.

5.5 Test communication and signals

5.5.1 General

Depending on the functionality of the Ethernet transceiver, different test signals are defined for communication in normal operation mode and wake-up from low power mode.

5.5.2 Test signals for normal operation mode

The communication test signal shall be used for testing Ethernet transceivers in normal operation mode. The parameters of this periodical signal are defined in Table 8.

Table 8 – Definition for transceiver mode configuration for normal operation mode

Topic	Content
Test communication	– data frame transmission initiated by host controller • Ethernet packet (e.g. ISO/IEC/IEEE 8802-3 Ethernet frame ,TCP/IP, UDP/IP…) with minimum 1000 byte data payload • minimum 80 % bus load • payload data $5A_{16}$ – data frame transmission initiated by Ethernet transceiver itself (optional) • activation of internal BIST or PRBS test with maximum possible performance

5.5.3 Test signals for low power mode

Tests of unwanted wake-up will be performed without test signal.

For test of wanted wake-up in low power mode, the definition of test communication in normal operation mode is used for initiate the wanted wake-up event for the DUT. Depending on the transceiver type, specific definitions for wanted wake-up events may exist. In this case, the definition of the semiconductor manufacturer is used.

5.6 Evaluation criteria

5.6.1 General

For immunity performance evaluation of Ethernet transceivers, different evaluation criteria are defined during and after exposure to disturbances.

The resulting functional status of the Ethernet transceiver shall be classified in status classes A_{IC}, C_{IC} or D_{IC} according to IEC 62132-1 following the definitions in 5.6.2.

5.6.2 Evaluation criteria for functional operation modes

The evaluation criteria for functional operation modes for Ethernet transceivers are defined in Table 9.

For failure monitoring, the evaluation criteria defined in Table 9 shall be used. The failure validation applies to all transceivers in the test network if not otherwise defined. As soon as a transceiver under test violates the evaluation criteria, an error event for this test case is generated. In case of monitoring analog signals, (e.g. INH output signal) the reference values depend on the transceiver under test and shall be captured in undisturbed conditions before the test. These reference signals combined with the boundary values are used to generate the failure validation masks. Deviations from the defined boundary values can be agreed and shall be noted in the test report.

Table 9 – Evaluation criteria for Ethernet transceiver

Transceiver mode	Purpose	Test signal	Function	Activity
Normal	Communi-cation and cross talk	Ethernet test communi-cation	Link	read out of register(s) for link status defined by the semiconductor manufacturer
			DTT	error check of all transferred data between the two nodes of the test network by microcontroller or FPGA or error check for BIST or PRBS test for data frame transmission initiated by Ethernet transceiver itself
			CRC	read out of available register for CRC status [a]
			SQI/SNR	read out and documentation of all available registers for indication of SQI or SNR value [b]
			RS-FEC	read out and documentation of available registers for indication of RS-FEC events [b]
			BIST or PRBS test [c]	read out of available register for status or result of BIST or PRBS tests
			other pin functions	function validation mask using maximum deviation defined by data sheet (e.g. INH)
Low power mode	unwanted wake-up	without	wake-up indication	function validation mask using maximum deviation defined by data sheet (e.g. INH)
	wanted wake-up [d]	link pulse	wake-up indication	function validation mask using maximum deviation defined by data sheet (e.g. INH)

Different evaluation criteria can be agreed for special cases and shall be noted in the test report.

[a] If no read out of required error registers at the transceiver is possible, the error validation shall be implemented into the microcontroller software in comparable way.

[b] Optional function, evaluation only if function is implemented.

[c] Optional function.
If a BIST or PRBS test is used instead of a data frame transmission, initiated by host controller, this evaluation replaces the CRC and DTT function.

[d] One transceiver (DUT) of the test network is configured as Slave and is set to low power mode. The second transceiver is configured as Master and will be set into normal mode for sending out link pulses to be detected as wake-up by the DUT. Only the DUT is monitored and shall wake up at least after 100 ms (see definition in ISO 21111-2).

5.6.3 Evaluation criteria in unpowered condition after exposure to disturbances

The input I-V characteristic (current versus voltage) of a pin under test to GND including mandatory components shall be measured using e.g. a semiconductor parameter analyzer. If measurements with mandatory components are not applicable they shall be removed. The test voltage range should cover or exceed the maximum voltage rating of the pin under test up to the level where e.g. break down, snap back or clamping occurs.

NOTE Commonly used test voltages are ± 50 V to ±70 V with test current limitations of ± 0,5 mA to ± 5 mA in order to avoid damage of IC during characteristic curve measurement.

Any significant change of I-V characteristic (e.g. more than ± 5 % of maximum applied test voltage or current) measured before and after the immunity test is considered as a failure. Figure 8 shows a principle drawing of the maximum deviation on an I-V characteristic.

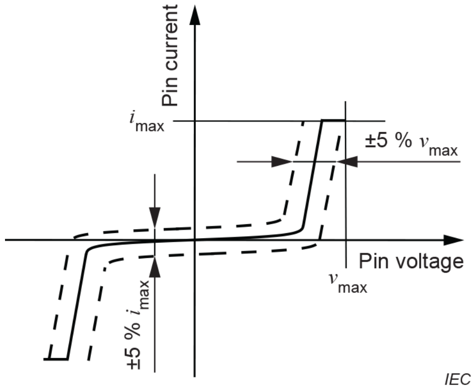


Figure 8 – Principle drawing of the maximum deviation on an I-V characteristic

Alternatively to the above described I-V characteristic test, a parameter test according to data sheet of the DUT can be used as well to verify damages of the IC.

5.6.4 Status classes

The functional status classes for Ethernet transceivers based on the evaluation criteria are defined in Table 10.

Table 10 – Definition of functional status classes

Resulting status class	Requirement
A_{IC}	– no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for Link, DTT, CRC and other pin functions in normal mode and wake-up indication in low power mode – no damage detected after exposure to disturbance, evaluation criteria of 5.6.3, that can be checked at the end of all functional tests
$A1_{IC}$	– no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for Link
$A2_{IC}$	– no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for DTT and CRC
$A3_{IC}$	– no error occurred during exposure to disturbance, evaluation criteria of 5.6.2 for unwanted wake-up caused by ESD discharges during exposure, proper wake-up functionality and correct change into normal mode on request during exposure
C_{IC}	– error occurred during exposure to disturbance, evaluation criteria of 5.6.2 – no error occurred after exposure to disturbance, evaluation criteria of 5.6.2, DUT automatically comes back into proper operation – no damage detected after exposure to disturbance, evaluation criteria of 5.6.3
D_{IC}	– error occurred during exposure to disturbance, evaluation criteria of 5.6.2 – no error occurred after exposure to disturbance, evaluation criteria of 5.6.2, but DUT does not automatically come back into proper operation when disturbance is removed until a simple operator action (e.g. re-initialization by MDIO or SPI ($D1_{IC}$), power off/on ($D2_{IC}$)) has been done – no damage detected after exposure to disturbance, evaluation criteria of 5.6.3

5.7 DUT specific information

The following information is required for setting up and conducting the EMC tests at Ethernet transceivers and shall be supported by the semiconductor manufacturer:

- test circuit for typical application of transceiver;
- software configuration data for setting the transceiver in typical application;
- detailed information for data transmission and error register read out activity.

The following additional information should be supported by the semiconductor manufacturer, if available or needed respectively:

- EMC optimized test circuit (optimized MDI test network and optimized filter or supplier specific filter at voltage supply pins);
- information for ESD protection devices;
- layout application hints or equivalent layout requirements;
- software configuration data for setting the transceiver in EMC optimized state.

6 Test and measurement

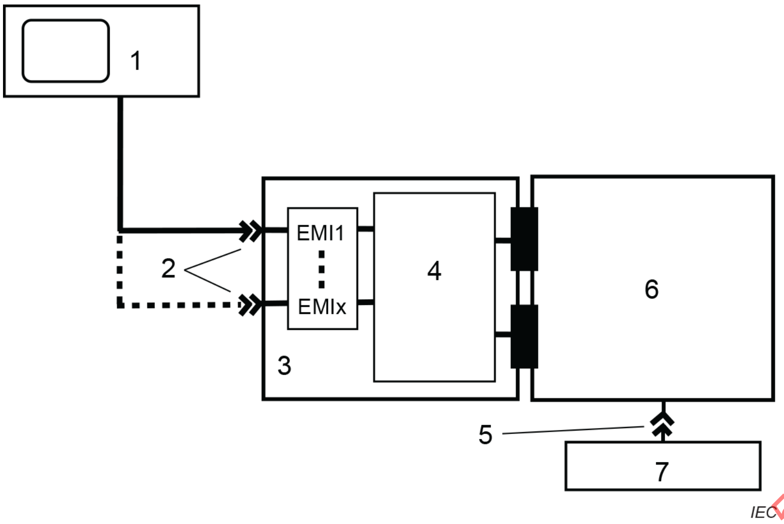
6.1 Emission of conducted RF disturbances

6.1.1 Test method

The measurement of the conducted RF emission shall be performed by 150 Ω direct coupling method according to IEC 61967-4.

6.1.2 Test setup

The conducted RF emission measurement of transceiver shall be carried out using a setup according to Figure 9 with the coupling network as defined in Table 6.



Key

1	Spectrum analyzer / EMI receiver	5	Connector
2	Coupling ports (MDI: EMI1, V_{BAT}: EMI2, WAKE: EMI3, V_{DDx}: EMIx), coaxial connector	6	Controller board
3	Test board	7	Power supply (V_{BAText}, V_{DDx_ext}, GND)
4	Test network		

Figure 9 – Test setup for measurement of conducted RF disturbances

The test equipment definitions are the following:

- spectrum analyzer / EMI receiver;
- test board;
- controller board;
- power supply.

6.1.3 Test procedure and parameters

The settings of the conducted RF measurement equipment are given in Table 11.

Table 11 – Settings of the conducted RF measurement equipment

RF Measurement equipment	Spectrum analyzer	EMI receiver
Detector	Peak	
Frequency range	0,15 MHz to 1 000 MHz (2 750 MHz optional)	
Resolution bandwidth (RBW) 150 kHz to 30 MHz: 30 MHz to 2 750 MHz:	 10 kHz 100 kHz	 9 kHz 120 kHz
Video bandwidth (VBW)	≥ 3 times RBW	–
Numbers of sweeps	10 (max hold)	–
Measurement time per step	–	≥ 100 ms
Frequency sweep time	≥ 100 s	–

RF Measurement equipment	Spectrum analyzer	EMI receiver
Frequency step width		
150 kHz to 30 MHz:	–	≤ 5 kHz
30 MHz to 2 750 MHz:	–	≤ 50 kHz
FFT based EMI receivers can be used as well if they meet CISPR 16-1-1 definitions.		

The conducted RF emission measurements shall be performed according to Table 12.

Table 12 – Conducted emission measurements

Transceiver mode	Coupling port [a]	Pin	MDI test network (BIN)	Ethernet system		
				1000BASE-T1	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	EMI1	MDI	Min-BIN	X	X	
			Std-BIN	X	X	
			Opt-BIN	X	X	X
	EMI1a,b		Std-BIN	X		
			Opt-BIN	X		
	EMI1c,d		Std-BIN	X	X	
			Opt-BIN	X	X	X
	EMI1e,f		Std-BIN		X	
			Opt-BIN		X	X
	EMI2 [b]	V_{BAT}	Opt-BIN	X	X	X
	EMI3 [b]	WAKE	Opt-BIN	X	X	X
	EMI4 [b]	V_{DDx}	Opt-BIN	X	X	X

X A test shall be performed.

[a] For definition of coupling ports see Table 6.

[b] For transceivers with different MII interfaces emission measurements at both nodes of the transceiver network with the MII configuration according to Table 5 are required. Alternatively the MII configuration for one node can be changed between the two defined MII interfaces for emission measurement.

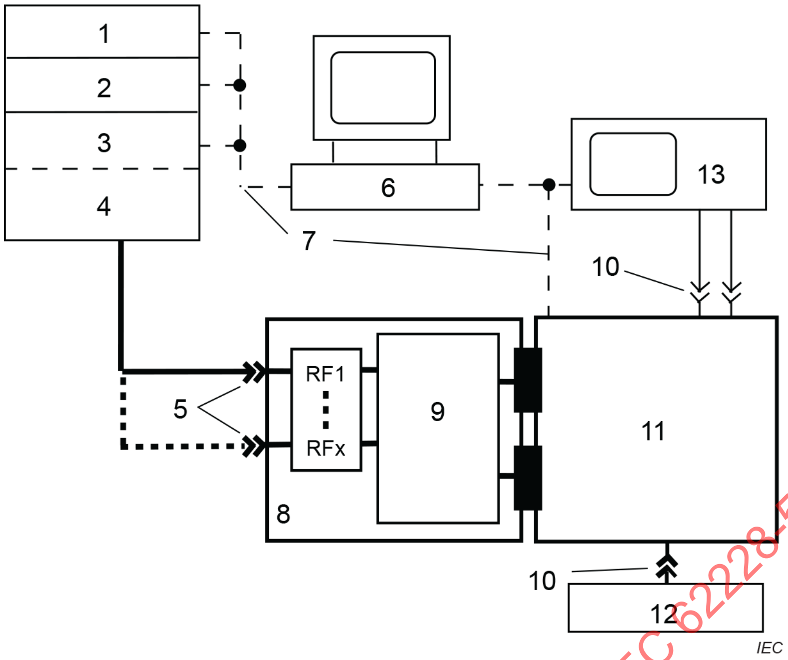
6.2 Immunity to conducted RF disturbances

6.2.1 Test method

The test of the conducted RF immunity shall be performed by using the DPI test method according to IEC 62132-4.

6.2.2 Test setup

The conducted RF immunity tests of transceiver shall be carried out using a setup according to Figure 10 with the coupling network as defined in Table 6.



Key

1	RF generator	8	Test board
2	RF amplifier	9	Test network
3	RF power meter	10	Connector
4	Directional coupler	11	Controller board
5	Coupling ports (MDI: RF1, V_{BAT}: RF2, WAKE: RF3), coaxial connector	12	Power supply (V_{BAText}, V_{DDx_ext}, GND)
6	Control PC (optional)	13	DSO
7	Remote control (optional)		

Figure 10 – Test setup for DPI tests

The test equipment definitions are the following:

- RF generator;
- RF amplifier (output power $P \geq 10$ W);
- power meter with directional coupler;
- test board;
- controller board;
- power supply;
- control PC (optional);
- digital storage oscilloscope (DSO, optional).

6.2.3 Test procedure and parameters

To determine the conducted RF immunity of the Ethernet transceiver, tests with the parameters given in Table 13 shall be carried out.

Table 13 – Specifications for DPI tests

Item	Parameter	
Frequency	Range	Step
	1 MHz to 10 MHz	0,25 MHz
	10 MHz to 100 MHz	1 MHz
	100 MHz to 200 MHz	2 MHz
	200 MHz to 400 MHz	4 MHz
	400 MHz to 1 000 MHz (2 000 MHz optional) [a]	10 MHz
Minimum forward power	10 dBm (10 mW)	
Maximum forward power	39 dBm (8 W)	
Power step size	0,5 dB	
Dwell time	1 s	
Modulation (including optional frequency ranges)	f = 1 MHz to 2 000 MHz: CW f = 1 MHz to 800 MHz: AM 80 % 1 kHz ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 806 MHz to 915 MHz: PM 217 Hz, ton 577 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 1 200 MHz to 1400 MHz: PM 300 Hz, ton 3 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 1 710 MHz to 1910 MHz: PM 217 Hz, ton 577 µs ($\hat{P}_{PM} = \hat{P}_{CW}$)	
Test procedure for evaluation of functional status class A_{IC}	Searching for malfunction during the complete dwell time while power is stepwise increased. An optimized control procedure can be used to reduce the test time but ensuring that there are no artifacts in the RF inputs during frequency or power steps. EXAMPLE: Procedure for each frequency step: – start with maximum forward power or with the level that caused a malfunction at the previous frequency step, – in case of malfunction at this power level reduce the power level by 6dB and repeat the test, – increase the power stepwise until a malfunction occurs or the maximum forward power is reached, – the immunity level at this frequency is the maximum forward power that causes no malfunction	
Test procedure for evaluation of functional status class C_{IC} or D_{IC}	Apply the test power for each frequency step and evaluate the functional status after each test.	

[a] Test up to f = 2000 MHz is optional and only recommended for coupling to MDI of 1000BASE-T1 transceivers. In this case the requirements of IEC 62132-4 for transfer characteristic of coupling network should also be fulfilled in this frequency range. For all other configurations tests up to f = 1 000 MHz are defined.

The tests for functional status class A_{IC} evaluation shall be performed according to Table 14.

For each test, an immunity threshold curve with the forward power as the parameter shall be determined and documented in a diagram in the test report.

Table 14 – DPI tests for functional status class A_{IC} evaluation of Ethernet transceivers

Transceiver mode	Coupling port [g]	Pin	MDI test network (BIN)	Failure validation for error / function					
				CRC, Link, DTT	SNR or SQI [f]	RS-FEC [f]	Sum [c]	Other pin function	Wake-up
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX					
normal mode / Ethernet test communi-cation	RF1	MDI	Min-BIN [a]				X/X/—		
			Std-BIN [b]				X/X/—		
			Opt-BIN [b]		X/X/X	X/—/—	X/X/X	X/X/X	
	RF1[a,b]		Std-BIN [b]				X/—/—		
			Opt-BIN [b]		X/—/—	X/—/—	X/—/—		
	RF1[c,d]		Std-BIN [b]				X/X/—		
			Opt-BIN [b]	X/—/—	—/X/X		X/X/X		
	RF1[e,f]		Std-BIN [b]				X/X/—		
			Opt-BIN [b]	—/X/X			X/X/—		
	RF2	V_{BAT}	Opt-BIN [a]				X/X/X	X/X/X	
	RF3	WAKE	Opt-BIN [a]				X/X/X	X/X/X	
low power mode / test of unwanted wakeup [d]	RF1	MDI	Min-BIN [a]						X/X/—
			Std-BIN [b]						X/X/—
			Opt-BIN [b]						X/X/X
	RF1[a,b]		Std-BIN [b]						X /—/—
			Opt-BIN [b]						X /—/—
	RF1[c,d]		Std-BIN [b]						X/X/—
			Opt-BIN [b]						X/X/X
	RF1[e,f]		Std-BIN [b]						X/X/—
			Opt-BIN [b]						X/X/—
	RF2	V_{BAT}	Opt-BIN [a]						X/X/X
	RF3	WAKE	Opt-BIN [a]						X/X/X

Transceiver mode	Coupling port [g]	Pin	MDI test network (BIN)	Failure validation for error / function					
				CRC, Link, DTT	SNR or SQI [f]	RS-FEC [f]	Sum [c]	Other pin function	Wake-up
low power mode / test of wanted wakeup [d,e]	RF1	MDI	Min-BIN [a]						X/X/–
			Std-BIN [b]						X/X/–
			Opt-BIN [b]						X/X/X
	RF1 [a,b]		Std-BIN [b]						X /–/–
			Opt-BIN [b]						X /–/–
	RF1 [c,d]		Std-BIN [b]						X/X/–
			Opt-BIN [b]						X/X/X
	RF1 [e,f]		Std-BIN [b]						X/X/–
			Opt-BIN [b]						X/X/–

X A test shall be performed.

[a] A test shall be done with CW and modulation (AM, PM), maximum test power 36 dBm.

[b] A test shall be done only with modulation (AM, PM), maximum test power 39 dBm.

[c] Sum error: Link, CRC, and DTT or Link and BIST / PRBS tests status evaluated in parallel.

[d] Test of wanted or unwanted wake up or Ethernet signal activity detection, depending on implemented function.

[e] One node is set to low power mode, a second node sends periodically a signal to be detected as wakeup by the node in low power mode.

[f] Documentation of SNR value (e.g. signal quality indicator or MSE value) or RS-FEC counter, if implemented. A test should be done for information only. There is no immunity limit defined.

[g] For a definition of coupling ports, see Table 6.

The tests for functional status class C_{IC} or D_{IC} shall be performed according to Table 15.

Table 15 – DPI tests for functional status class C_{IC} or D_{IC} evaluation of Ethernet transceivers

Transceiver mode	Coupling port	Pin	MDI test network (BIN)	Failure validation for error / function
				Sum [c]
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX
normal mode / Ethernet test communi-cation	RF1 [a]	MDI	Opt-BIN	X/X/X
	RF2 [b]	V_{BAT}	Opt-BIN	X/X/X
	RF3 [b]	WAKE	Opt-BIN	X/X/X

X A test shall be performed.

[a] A test shall be done with modulation (AM, PM), maximum test power 39 dBm.

[b] A test shall be done with CW, maximum test power 36 dBm.

[c] Sum error: CRC, Link and DTT evaluated in parallel.

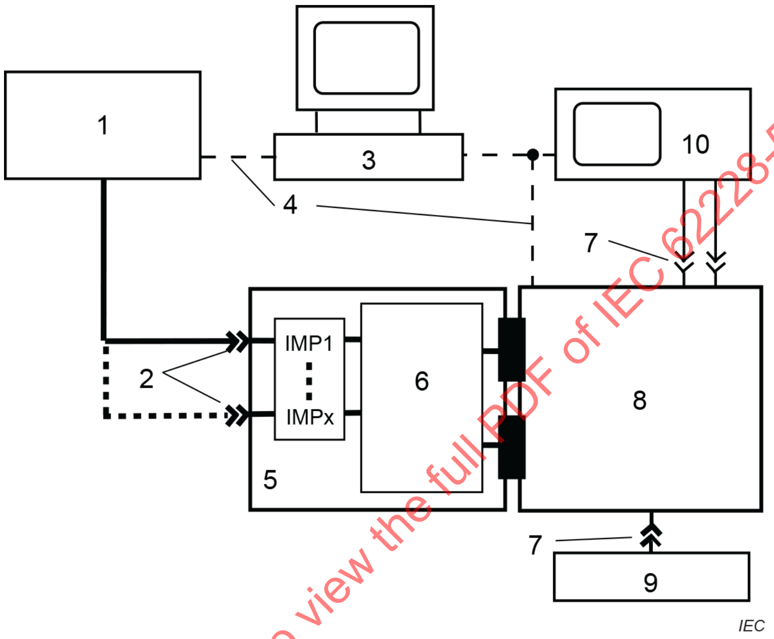
6.3 Immunity to impulses

6.3.1 Test method

The test of the impulse immunity shall be performed by using the non-synchronous transient injection method according to IEC 62215-3.

6.3.2 Test setup

The impulse immunity tests of transceiver shall be carried out using a setup according to Figure 11 with the coupling network as defined in Table 6.



Key

1	Test pulse generator	6	Test network
2	Coupling ports (MDI: IMP1, V_{BAT}: IMP2, WAKE: IMP3), coaxial connector	7	Connector
3	Control PC (optional)	8	Controller board
4	Remote control (optional)	9	Power supply (V_{BAText}, V_{DDx_ext}, GND)
5	Test board	10	DSO

Figure 11 – Test setup for impulse immunity tests

The test equipment definitions are the following:

- test pulse generator (according to ISO 7637-2);
- test board;
- controller board;
- power supply;
- control PC (optional);
- digital storage oscilloscope (DSO, optional).

6.3.3 Test procedure and parameters

To determine the immunity of the transceiver against impulses defined in ISO 7637-2, tests with the definitions and parameters given in Table 16 and Table 17 shall be performed.

Table 16 – Specifications for impulse immunity tests

Item	Definitions and parameters
Test pulses (see Table 17)	1, 2a, 3a, 3b at coupling port IMP2: test pulse generator provides impulses and voltage supply V_{BAT} for DUT 3a, 3b, (1, 2a optional) at coupling port IMP1, IMP3: test pulse generator provides impulses but no voltage supply
Amplitude step size	10 V
Dwell time	1 min for tests of functional status class A_{IC} 10 min for tests of functional status class C_{IC} or D_{IC}
Test procedure for functional status class A_{IC}	Searching for malfunction during a dwell time of minimum 5 s while pulse amplitude is stepwise increased up to the defined test pulse levels (as e.g. given in Table D.4). At the determined maximum voltage the achieved immunity level shall be proved with a dwell time of 1 min. An optimized control procedure can be used to reduce test time. The immunity level is the maximum amplitude that causes no malfunction.
Test procedure for functional status class C_{IC} or D_{IC}	Apply the defined test pulses (as e.g. given in Table D.4) and evaluate the functional status after each test.

Table 17 – Parameters for impulse immunity test

Test pulse [a]	Maximum pulse amplitude $V_{s\ max}$ V	Pulse repetition frequency $(1/t_1)$ Hz	Internal resistance R_i Ω	Remarks
1	− 100	2	10	battery shall be off only during the pulse
2a	+ 75	2	2	–
3a	− 150	10 000	50	–
3b	+ 100	10 000	50	–

[a] according to ISO 7637-2, pulse amplitudes are defined under open load conditions, parameters for rise time and duration for 12 V- systems are set as default. Other pulse values for target applications in other power domains as e.g. 24 V or pulses defined in IEC standards (e.g. IEC 61000-4-4 and IEC 61000-4-5) can be used if required for the transceiver application.

The tests for functional status class A_{IC} evaluation shall be performed according to Table 18. For each test an impulse immunity level shall be determined and documented in the test report.

Table 18 – Impulse immunity tests for functional status class A_{IC} evaluation of Ethernet transceivers

Transceiver mode	Coupling port [e]	Pin	MDI test network (BIN)	Failure validation for error / function					
				CRC, Link, DTT	SNR [d]	RS-FEC [d]	Sum [a]	Other pin function	Wake-up
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX					
normal mode / Ethernet test communi-cation	IMP1	MDI	Min-BIN				X/X/—		
			Std-BIN				X/X/—		
			Opt-BIN	X/X/X	X/X/X	X /—/—	X/X/X	X/X/X	
	IMP2	V_{BAT}	Opt-BIN				X/X/X	X/X/X	
	IMP3	WAKE	Opt-BIN				X/X/X	X/X/X	
low power mode / test of unwanted wakeup [b]	IMP1	MDI	Min-BIN						X/X/—
			Std-BIN						X/X/—
			Opt-BIN						X/X/X
	IMP2	V_{BAT}	Opt-BIN						X/X/X
	IMP3	WAKE	Opt-BIN						X/X/X
low power mode / test of wanted wakeup [b,c]	IMP1	MDI	Min-BIN						X/X/—
			Std-BIN						X/X/—
			Opt-BIN						X/X/X

X A test shall be performed.

[a] Sum error: Link, CRC, and DTT or Link and BIST / PRBS tests status evaluated in parallel.

[b] Test of wanted or unwanted wake up or Ethernet signal activity detection, depending on implemented function.

[c] One node is set to low power mode, a second node sends periodically a signal to be detected as wakeup by the node in low power mode.

[d] Documentation of SNR value (e.g. signal quality indicator or MSE value) or RS-FEC counter, if implemented. Test should be done for information only. There is no immunity limit defined.

[e] For a definition of coupling ports, see Table 6.

The tests for functional status class C_{IC} or D_{IC} shall be performed according to Table 19.

Table 19 – Impulse immunity tests for functional status class C_{IC} or D_{IC} evaluation of Ethernet transceivers

Transceiver mode	Coupling port [b]	Pin	MDI test network (BIN)	Failure validation for error / function
				Sum [a]
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX
normal mode / Ethernet test communi-cation	IMP1	MDI	Opt-BIN	X/X/X
	IMP2	V_{BAT}	Opt-BIN	X/X/X
	IMP3	WAKE	Opt-BIN	X/X/X

X A test shall be performed.

[a] Sum error: CRC, Link and DTT evaluated in parallel.

[b] For a definition of coupling ports, see Table 6.

6.4 Electrostatic Discharge (ESD)

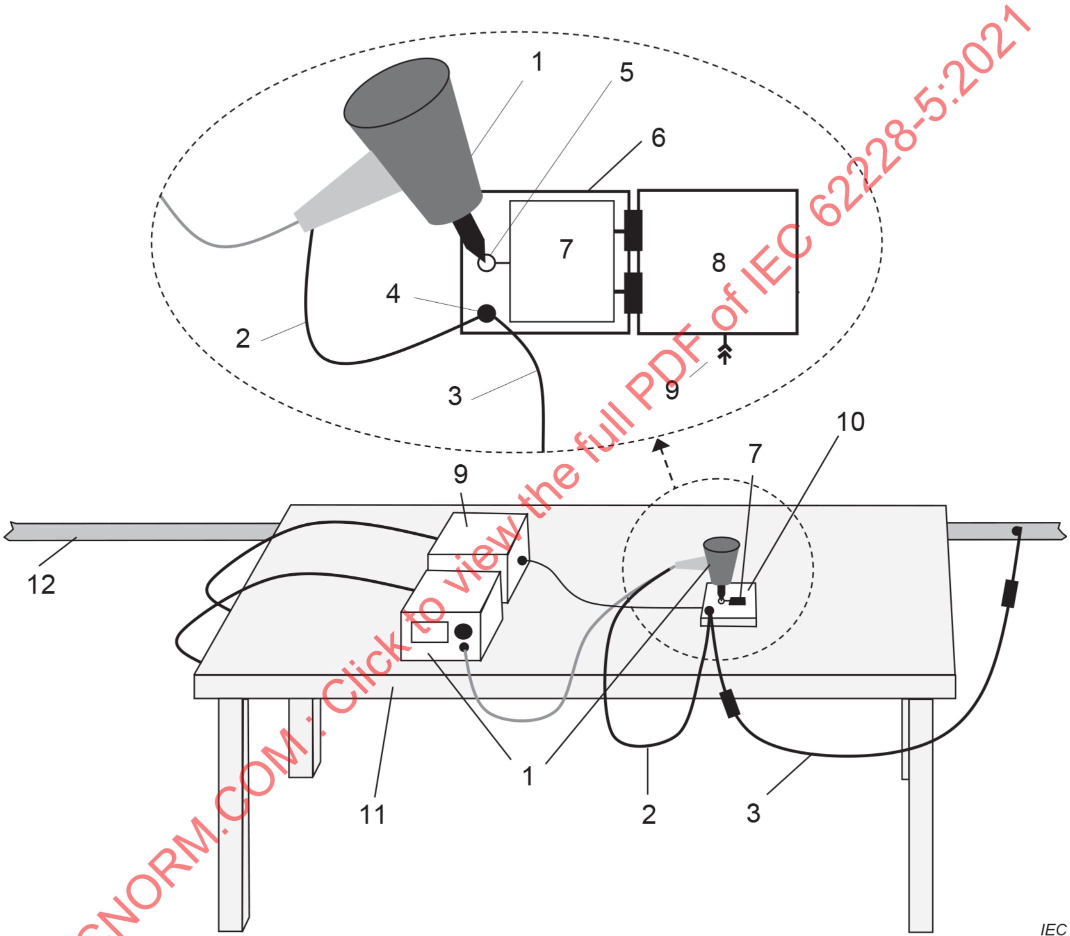
6.4.1 Test method

The ESD immunity test shall be performed in powered and unpowered mode by using the direct discharge method according to ISO 10605.

6.4.2 Test setup

6.4.2.1 Test setup for powered test

ESD tests in powered mode of Ethernet transceivers shall be carried out using a test setup according to Figure 12 and Figure 13.



Key

1	ESD generator	7	Test network
2	ESD generator ground return cable	8	Controller board
3	Connection to protective earth including two 470 kΩ resistors on both ends	9	Monitoring and stimulation, power supply
4	Ground plane connection point of powered ESD test board	10	Powered ESD test board with controller board
5	Discharge point	11	Nonmetallic table
6	Powered ESD test board	12	Protective earth

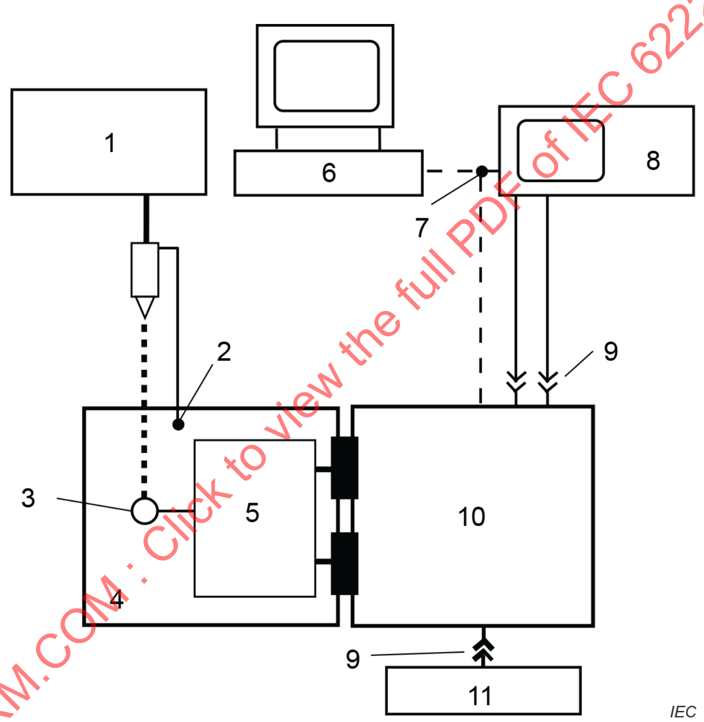
Figure 12 – Test setup for powered ESD tests – principle arrangement

The test equipment definitions for powered ESD tests are the following:

- ESD generator (according to ISO 10605, discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω);
- powered ESD test board;
- controller board;
- auxiliary equipment as power supply, monitoring and stimulation (optional, only needed for tests in powered mode and functional pre/post validation).

The ESD generator ground return cable shall be directly connected to ground plane of the powered ESD test board. This point shall be connected to protective earth of the electrical grounding system of the test laboratory. An optional ground plane with a minimum size of 0,5 m × 0,5 m can be used but shall be also connected to protective earth.

The tip of the ESD generator shall be directly contacted with the discharge point ESD1 IND of the powered ESD test board (described in Annex B) for testing.



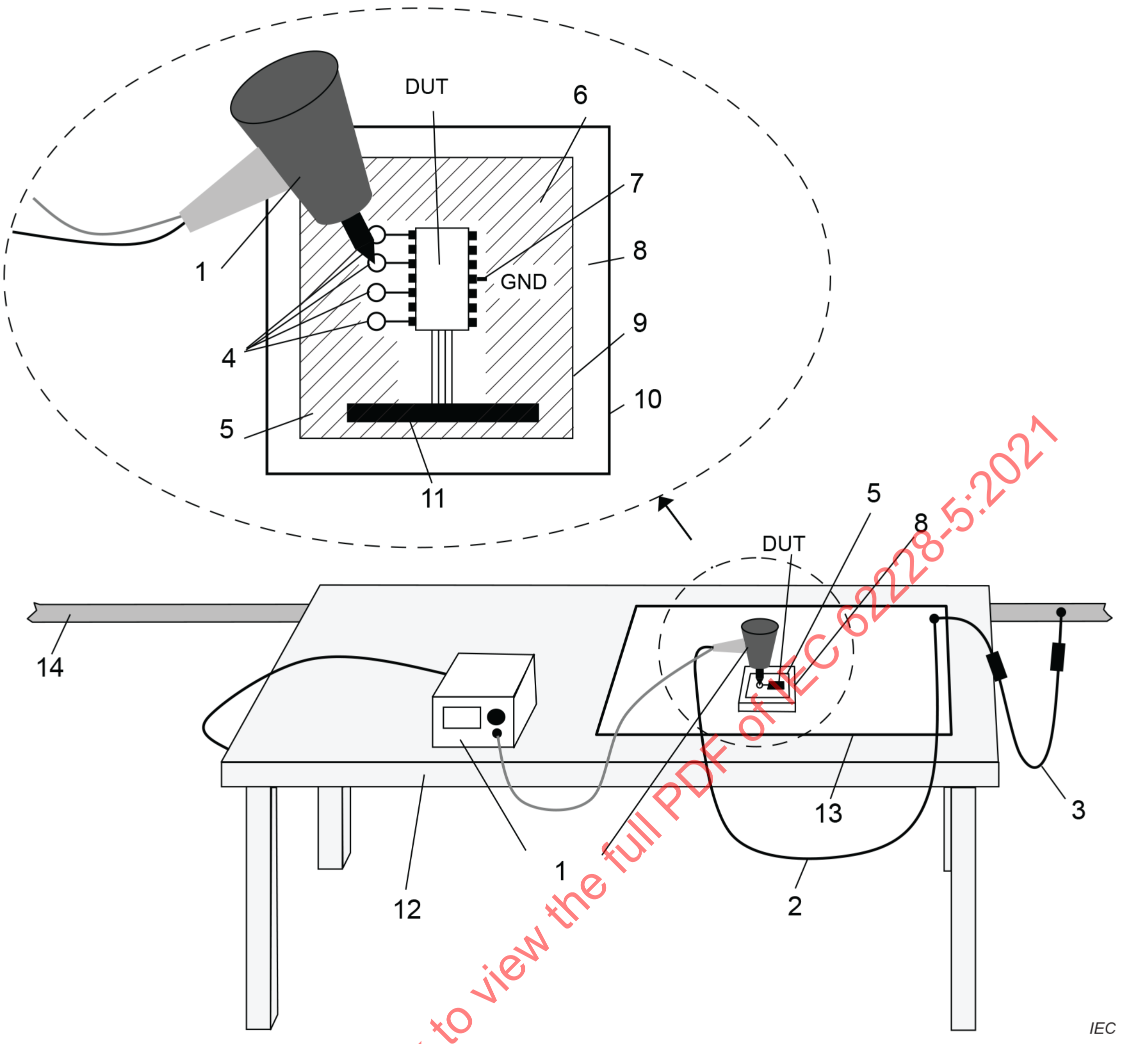
Key

1	ESD generator	7	Remote control (optional)
2	Ground return connection	8	DSO (optional)
3	Coupling port (MDI: ESD1 IND)	9	Connector
4	Powered ESD test board	10	Controller board
5	Test network	11	Power supply (V_{BAText}, V_{DDx_ext}, GND)
6	Control PC (optional)		

Figure 13 – Test setup for powered ESD tests – stimulation and monitoring

6.4.2.2 Test setup for unpowered test

ESD tests in unpowered mode of Ethernet transceivers shall be carried out using a test setup according to Figure 14 for ESD tests itself and according to Figure 15 for function validation pre and post ESD test.



Key

1	ESD generator	8	Metallic test fixture
2	ESD generator ground return cable	9	Surface connection ground plane of ESD test board to metallic test fixture
3	Connection to protective earth including two 470 kΩ resistors on both ends	10	Surface connection of metallic test fixture to ground plane
4	Discharge points	11	Connector to monitoring and stimulation
5	ESD test board	12	Nonmetallic table
6	Ground plane of ESD test board	13	Ground plane
7	Connection pin GND to ground plane of ESD test board	14	Protective earth

Figure 14 – Test setup for unpowered ESD tests – principle arrangement

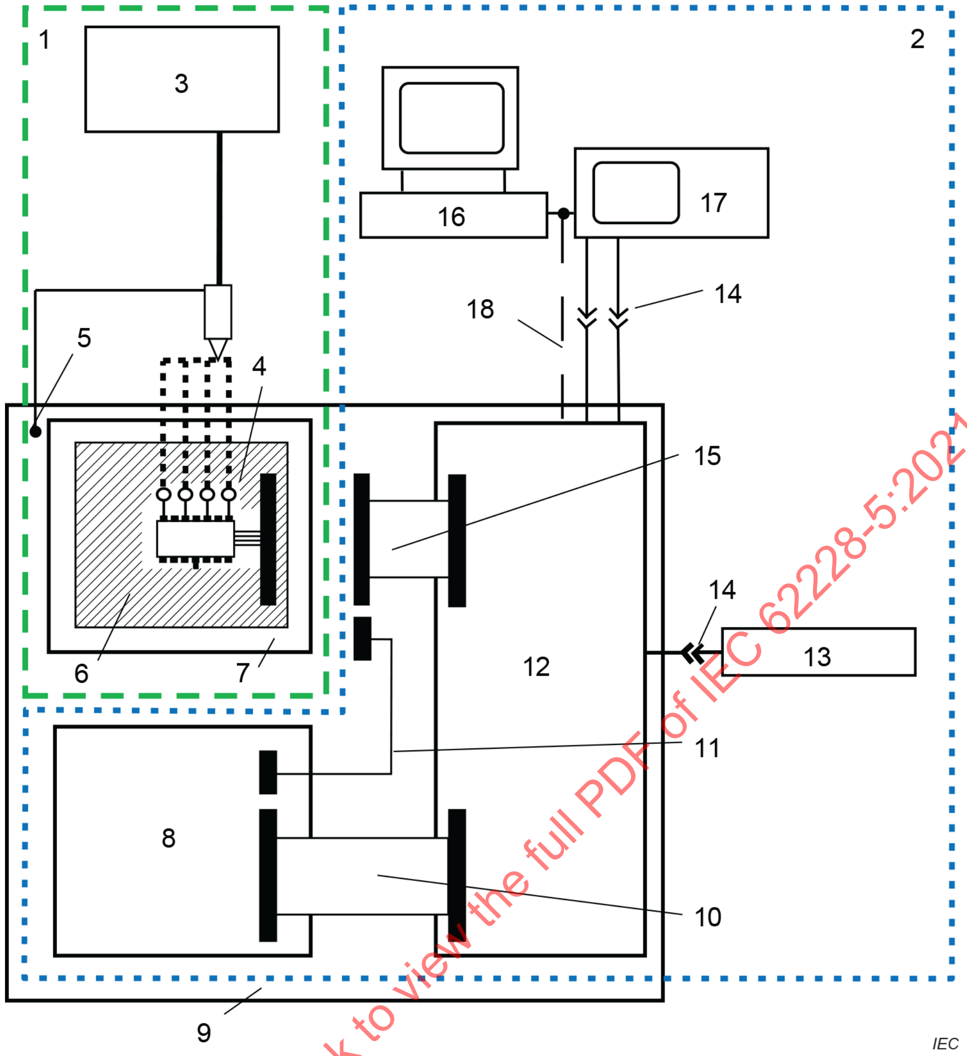
The test equipment definitions for unpowered ESD tests are the following:

- ESD generator (according to ISO 10605, discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω);
- ESD test board;
- test fixture;
- ground plane.

The ground plane with a minimum size of 0,5 m × 0,5 m shall be connected to protective earth of the electrical grounding system of the test laboratory. The ESD generator ground return cable shall be directly connected to this ground plane.

The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The ground connection of the test fixture shall be connected to ground plane with low impedance and low inductance. This surface connection should have a contact area of at least 4 cm^2. Copper tapes can be used in addition.

The tip of the ESD generator shall be directly contacted with one of the discharge points ESD1a, ESD1b, ESD2 and ESD3 of the ESD test board (described in Annex B) for testing.



Key

1	ESD Generation and Coupling	10	Interface to link partner
2	Monitoring and Stimulation (only used for functional validation pre and post ESD test)	11	MDI interface
3	ESD generator	12	Controller board
4	Coupling ports (MDIP: ESD1a, MDIN: ESD1b, V_{BAT}: ESD2, WAKE: ESD3)	13	Power supply (V_{BAText}, V_{DDx_ext}, GND)
5	Ground return connection	14	Connector
6	ESD test board	15	Controller interface
7	Metallic test fixture	16	Control PC (optional)
8	Ethernet link partner	17	DSO (optional)
9	Ground plane	18	Remote control (optional)

Figure 15 – Test setup for unpowered ESD tests – stimulation and monitoring for function validation pre and post ESD test

The test equipment definitions for function validation pre and post ESD test are the following:

- ESD test board;
- test fixture;
- controller board;

- board with Ethernet link partner (test board as used for RF emission, DPI and transient tests is proposed), and
- auxiliary equipment as power supply, monitoring and stimulation.

For tests in unpowered mode, the interfaces between ESD test board and controller board (controller interface) and ESD test board and Ethernet link partner (MDI interface) are disconnected during test. For functional pre and post validation they are connected.

6.4.3 Test procedure and parameters

To determine the ESD robustness of the Ethernet transceiver, tests shall be carried out with the parameters given in Table 20.

Table 20 – Specifications for ESD tests

Item	Parameter
Type of discharge	contact
Discharge circuit	R = 330 Ω, C = 150 pF
Discharge voltage levels and voltage steps for powered ESD tests	start level: 0,5 kV stop level: V_{ESD_damage} or 8 kV voltage step: 0,5 kV, 1 kV (starting at V_{ESD} = 1 kV)
Discharge voltage levels unpowered ESD tests	start level: 1 kV stop level: V_{ESD_damage} or 15 kV voltage step: 1 kV

The tests in powered mode for functional status class A_{IC}, C_{IC} and D_{IC} evaluation shall be performed according to Table 21. For each test, an ESD immunity level shall be determined and documented in the test report.

Table 21 – ESD tests in powered mode for functional status class A_{IC}, C_{IC} and D_{IC} evaluation of Ethernet transceivers

Transceiver mode	Coupling port [a]	Pin	MDI test network (BIN)	Failure validation for status class				
				$A1_{IC}$ (Link error)	$A2_{IC}$ (CRC, DTT error)	$A3_{IC}$ (unwanted wake up)	C_{IC}	D_{IC}
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX				
Test sequence from low power mode to normal mode	ESD1 IND	MDI	Opt-BIN	X/X/X				

X A test shall be performed with a minimum of 3 DUTs according to the following procedure:

1) disconnect DUT from power supply;
2) perform a reference measurement for the I/V characteristic curve (pin to GND) on all MDI pins;
3) connect DUT to power supply and set it to low power mode;
4) perform 3 discharges with positive polarity on discharge pad DP IND with 5 s delay between the discharges with evaluation of function status class $A3_{IC}$ according to Table 10 during test;
5) send wake-up signal by Ethernet link partner and check for proper wake-up function;
6) set DUT to normal mode with Ethernet test communication;
7) perform a reference test for proper function;
8) perform 3 discharges with positive polarity on discharge pad DP IND with 5 s delay between the discharges with evaluation of function status classes $A1_{IC}$, $A2_{IC}$ and C_{IC} according to Table 10 during test;
9) disconnect DUT from power supply;
10) connect the pin or discharge pad to the ground reference plane via a 1 MΩ resistor to ensure zero potential on the pin;
11) perform the I/V characteristic curve measurement (tested pin to GND) and failure validation of function status classes DIC according to Table 10;
12) proceed with point 1) to 11) with negative polarity;
13) proceed with point 1) to 12) with the next higher ESD test voltage up to damage of the tested pin or maximum defined ESD test level is reached.

[a] For a definition of coupling ports, see Table 7.

The tests in unpowered mode for functional status class D_{IC} evaluation shall be performed according to Table 22. For each test, an ESD immunity level shall be determined and documented in the test report.

Table 22 – ESD tests in unpowered mode for functional status class D_{IC} evaluation of Ethernet transceiver ICs

Transceiver mode	Coupling port [a]	Pin	MDI test network (BIN)	Failure validation for status class D_{IC}
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX
Unpowered	ESD1a, ESD1b	MDI	Min-BIN	X/X/–
			Std-BIN	X/X/–
			Opt-BIN	X/X/X
	ESD2	V_{BAT}	Opt-BIN	X/X/X
	ESD3	WAKE	Opt-BIN	X/X/X

X A test shall be performed with a minimum of 3 transceiver according to the following procedure:

1) perform reference test for proper function (check sum error) while connecting DUT to power supply and set it to normal mode;
2) perform a reference measurement for the I/V characteristic of all pins to be tested (pin to GND);
3) apply 3 ESD pulses with positive polarity on discharge point ESD2 (VBAT) with 5 s delay in between, after each single ESD pulse the pin or discharge point should be discharged to the ground to ensure zero potential before the next ESD pulse;
4) perform failure validation;
5) proceed with points 3) to 4) with discharge points ESD3 (WAKE);
6) proceed with points 3) to 4) with discharge points ESD1a (MDIP);
7) proceed with points 3) to 4) with discharge points ESD1b (MDIN);
8) proceed with point 3) to 7) with negative polarity;
9) proceed with point 3) to 8) with the next higher ESD test voltage up to damage of the tested pin or maximum defined ESD test level is reached;

   If one pin is damaged, a new IC should be used to continue the test of the other pins.

[a] For definition of coupling ports, see Table 7.

7 Test report

The following items should be included in the test report:

- schematic diagram of test configurations;
- failure criteria, used at immunity tests;
- picture or drawing of test circuit boards;
- transfer characteristics of coupling and decoupling networks;
- description of test equipment;
- description of the software configuration;
- description of any deviation from previously defined test parameter;
- test results.

Annex A
(normative)

Ethernet test circuits

A.1 General

The Ethernet test circuits define the details of the complete test circuitry for testing Ethernet transceivers in functional operating modes under network condition and for a single transceiver for ESD. They define mandatory components and optional components for Ethernet transceiver functions and components for coupling networks, decoupling networks which are used for power supply, stimulation, monitoring and testing of the DUT.

The Ethernet test circuit is basic for the test results and their interpretation.

A.2 Test circuit for Ethernet transceivers for functional tests

A general drawing of the test circuit diagram of the Ethernet test network for testing 100BASE-T1 and 1000BASE-T1 Ethernet transceivers in functional operating modes for conducted tests is given in Figure A.1. A general drawing of the conducted test circuit diagram for testing 100BASE-TX Ethernet transceivers is given in Figure A.2.

A 100BASE-T1 and 1000BASE-T1 Ethernet node consists of transceiver (A10, A20) with external mandatory components (X11, X12, X13, X14, X21, X22, X23, X24) and the BIN (L11, L21, C12, C13, C22, C23, R11, R12, R13, R21, R22, R23, C11, C21) and decoupling networks at monitored pins (R16, R26).

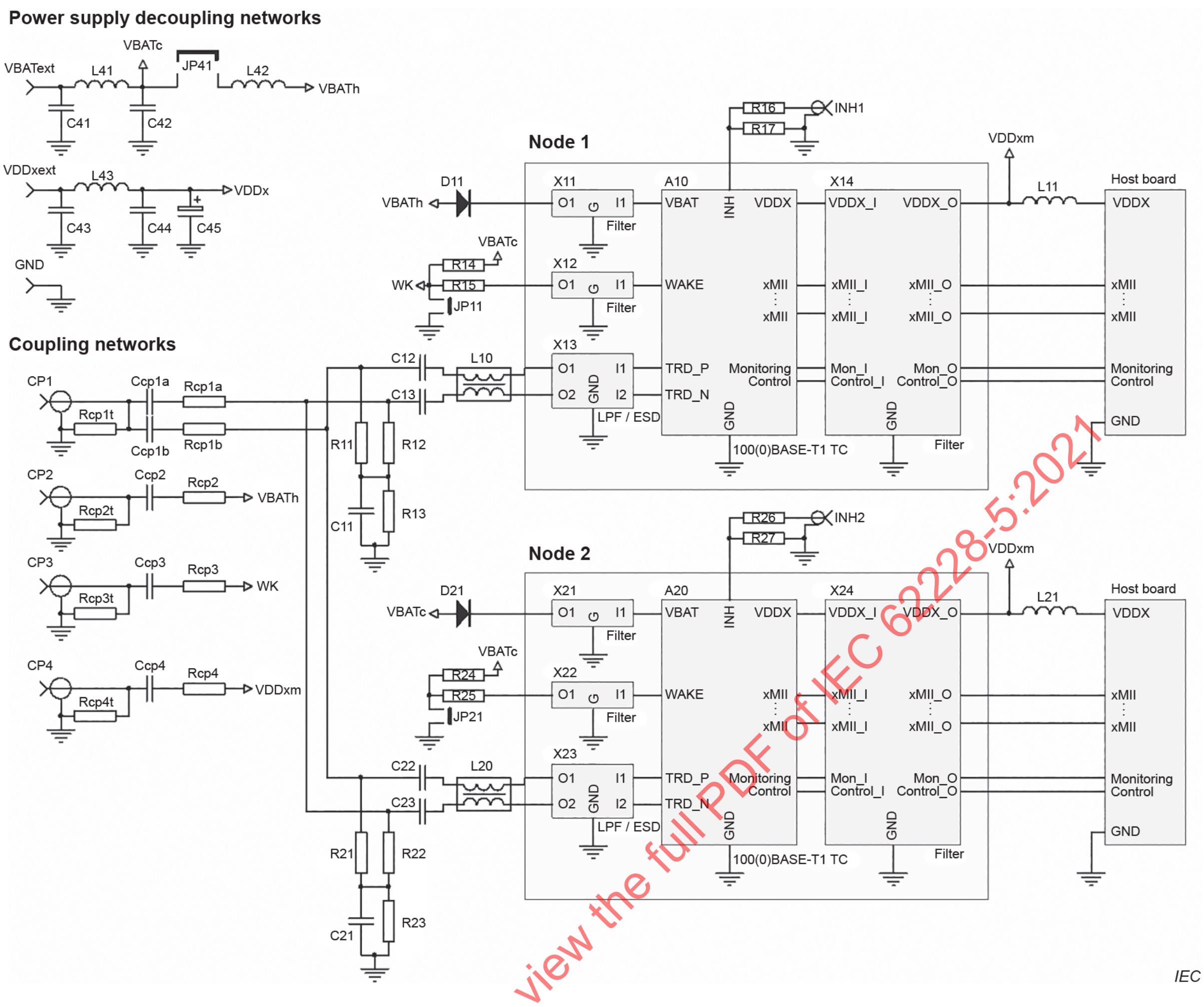
All external mandatory components (except components for MDI) shall be used according to the specification of the Ethernet transceiver. If special components for MDI are defined in the specification, this circuitry should be tested in addition.

The resistor values at the WAKE pin shall be set to the maximum specified value (default R = 3,3 kΩ) for R14, R24 and to the minimum specified value (default R = 33 kΩ) for R15, R25.

For RF decoupling of monitored pins INH, the default resistor value is set to R = 1 kΩ for all tests.

In order to avoid a floating voltage at pin INH in sleep mode, a pull down resistor (R17, R27) shall be used with values according to the IC specifications (default R = 10 kΩ).

For decoupling of external power supplies, two-stage LC-filters (L41, L42, C41, C42 and L43, C43, C44, C45) are used separately for V_{BAT} and V_{DDx}. The impedance of L42 should be greater than 400 Ω in the frequency range of interest. Jumper JP41 is opened to disconnect the supply voltage and the RF decoupling filter network at V_{BAT} during the impulse tests at V_{BAT}. In this case, the voltage supply V_{BAT} is directly provided via the IMP2 coupling network.

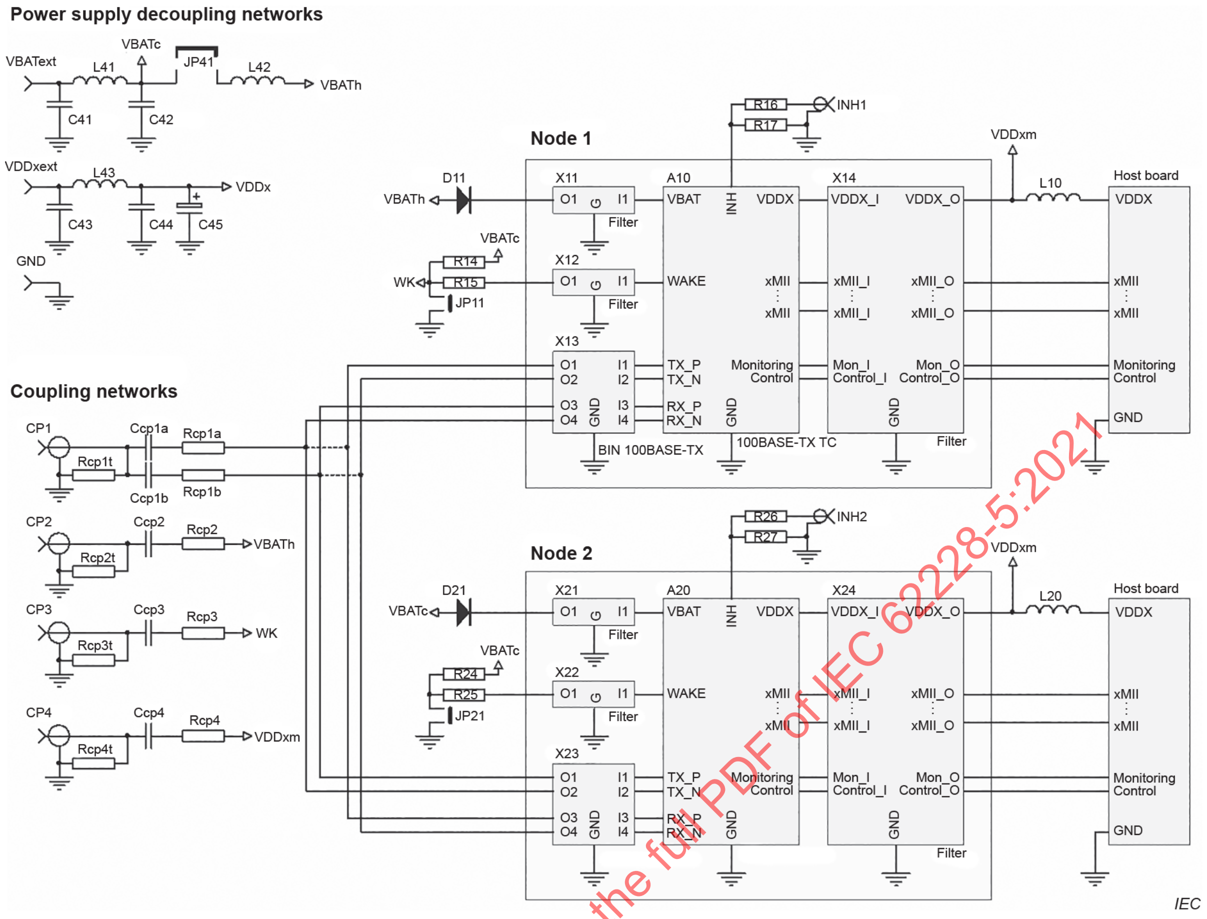


Key

Components

A10, A20	Ethernet transceiver 100BASE-T1 or 1000BASE-T1
C11, C21	capacitor C = 4,7 nF (default value, placement depend on test case)
C12, C13, C22, C23	capacitor C = 100 nF
C41, C43, C46	capacitor C = 1 nF
C42, C44, C47	capacitor C = 330 pF
C45	capacitor C = 22 µF
Ccp1a, Ccp1b, Ccp2, Ccp3, Ccp4	capacitor (value dependent on test)
D11, D21	diode, general purpose rectifier type
JP11, JP21	Jumper
L10, L20	Common mode choke which satisfying the requirements in Annex E (placement depend on test case)
L11, L21	inductor L = 4,7 µH (only populated for emission measurements at V_{DDx})
L41, L43	inductor L = 47 µH
L42	impedance should be greater than 400 Ω in the frequency range of interest
R11, R12, R21, R22	resistor R = 1 kΩ (± 1 % for 100BASE-T1, ± 0,5 % for 1000BASE-T1, default value, placement depend on test case)
R13, R23	resistor R = 100 kΩ (default value, placement depend on test case)
R14, R24	resistor R = 3,3 kΩ
R15, R25	resistor R = 33 kΩ
R16, R26	resistor R = 1 kΩ
R17, R27	resistor R = 10 kΩ
Rcp1a, Rcp1b, Rcp2, Rcp3, Rcp4	resistor (value dependent on test)
Rcp1t, Rcp2t, Rcp3t, Rcp4t	resistor (value dependent on test)
X11, X12, X13, X14, X21, X22, X23, X24	Filter network or external circuitry defined by semiconductor manufacturer

Figure A.1 – General drawing of the circuit diagram of test network for 100BASE-T1 and 1000BASE-T1 Ethernet transceivers for functional test using conducted test methods



Key

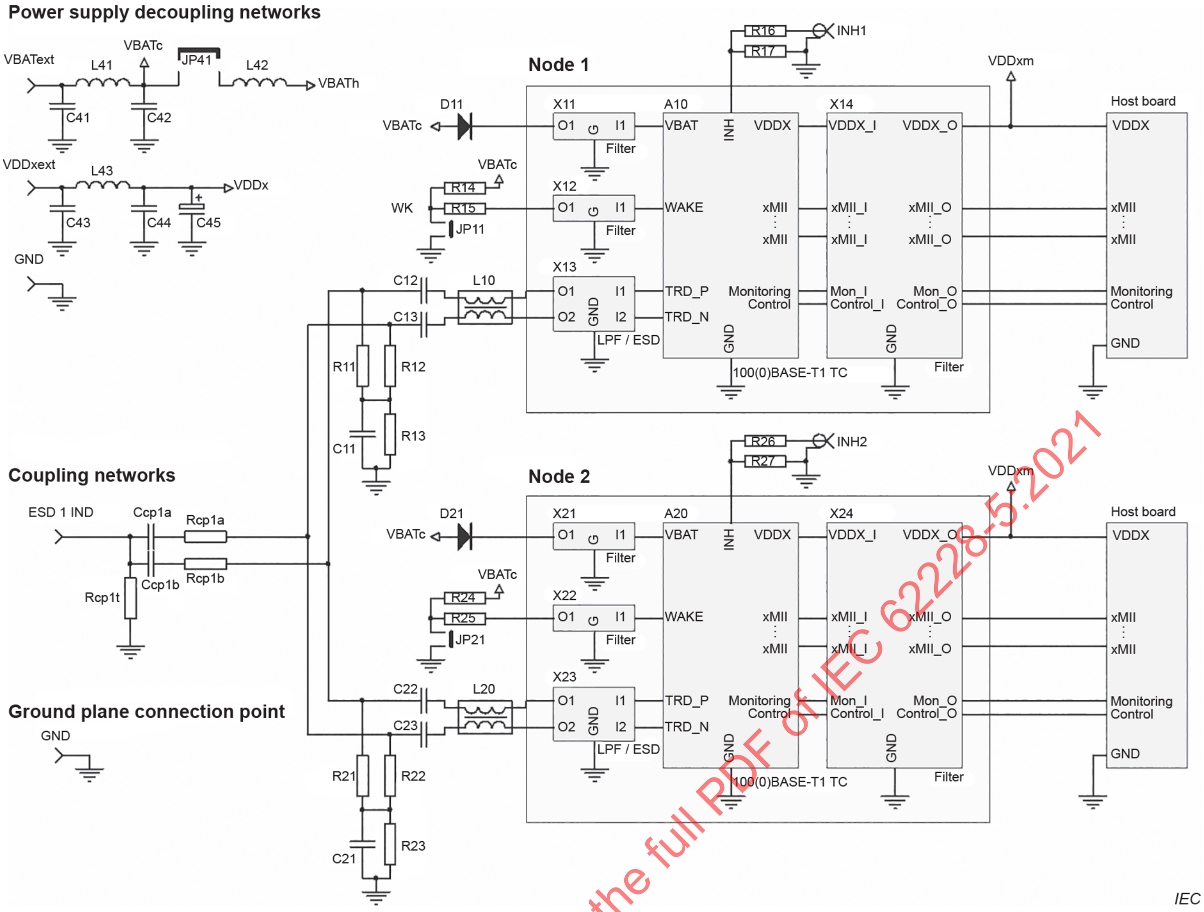
Components

A10, A20	Ethernet transceiver 100BASE-TX
C41, C43	capacitor C = 1 nF
C42, C44	capacitor C = 330 pF
C45	capacitor C = 22 µF
Ccp1a, Ccp1b, Ccp2, Ccp3, Ccp4	capacitor (value dependent on test)
D11, D21	diode, general purpose rectifier type
JP11, JP21	Jumper
L10, L20	inductor L = 4,7 µH (only populated for emission measurements at V_{DDx})
L41, L43	inductor L = 47 µH
L42	impedance should be greater than 400 Ω in the frequency range of interest
R14, R24	resistor R = 3,3 kΩ
R15, R25	resistor R = 33 kΩ
R16, R26	resistor R = 1 kΩ
R17, R27	resistor R = 10 kΩ
Rcp1a, Rcp1b, Rcp2, Rcp3, Rcp4	resistor (value dependent on test)
Rcp1t, Rcp2t, Rcp3t, Rcp4t	resistor (value dependent on test)
X11, X12, X14, X21, X22, X24	Filter network or external circuitry defined by semiconductor manufacturer
X13, X23	Specific BIN defined by semiconductor manufacturer for 100BASE-TX mode (e.g. magnetics, termination, LPF)

Figure A.2 – General drawing of the circuit diagram of test network for 100BASE-TX Ethernet transceivers for functional test using conducted test methods

A.3 Test circuit for Ethernet transceivers for ESD test

A general drawing of the test circuit diagram for testing immunity against ESD of Ethernet transceivers is given for powered mode in Figure A.3 and for unpowered mode in Figure A.4.



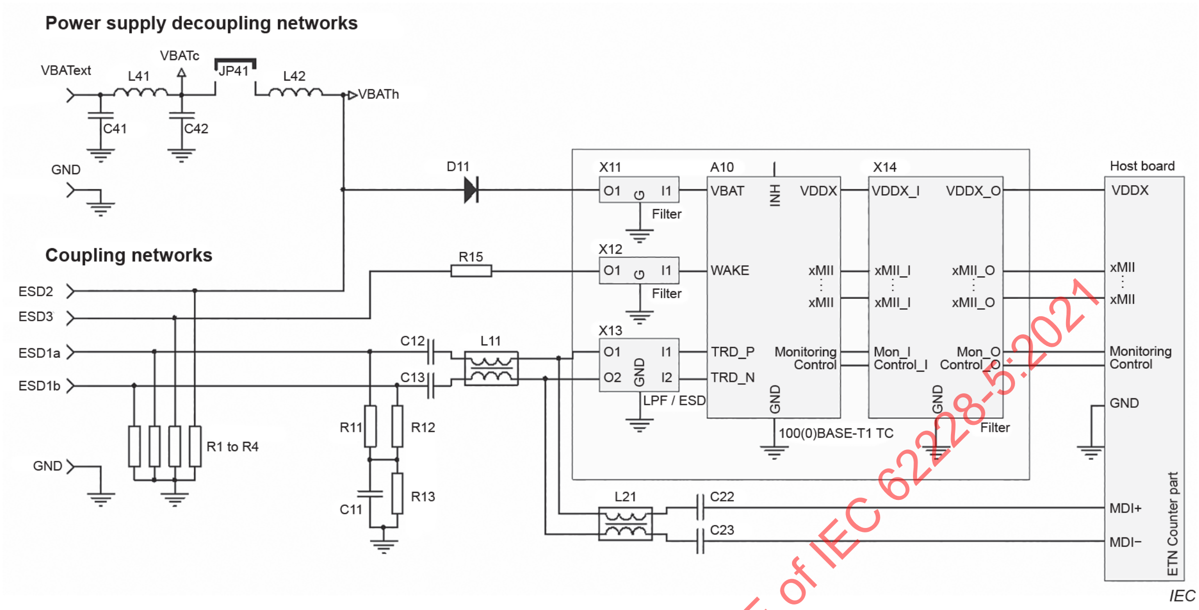
Key

Components

A10, A20	Ethernet transceiver 100BASE-TX
C11, C21	capacitor C = 4,7 nF (default value, placement depend on test case)
C12, C13, C22, C23	capacitor C = 100 nF
C41, C43	capacitor C = 1 nF
C42, C44	capacitor C = 330 pF
C45	capacitor C = 22 µF
Ccp1a, Ccp1b	capacitor C = 33 pF
D11, D21	diode, general purpose rectifier type
JP11, JP21	Jumper
L10, L20	Common mode choke which satisfying the requirements in Annex E (placement depend on test case)
L41, L43	inductor L = 47 µH
L42	impedance should be greater than 400 Ω in the frequency range of interest
R11, R12, R21, R22	resistor R = 1 kΩ (± 1 % for 100BASE-T1, ± 0,5 % for 1000BASE-T1, default value, placement depend on test case)
R13, R23	resistor R = 100 kΩ (default value, placement depend on test case)
R14, R24	resistor R = 3,3 kΩ
R15, R25	resistor R = 33 kΩ
R16, R26	resistor R = 1 kΩ
R17, R27	resistor R = 10 kΩ
Rcp1a, Rcp1b	resistor R = 120 Ω
Rcp1t	resistor R = 220 kΩ
X11, X12, X14, X21, X22, X24	Filter network or external circuitry defined by semiconductor manufacturer
X13, X23	Specific BIN defined by semiconductor manufacturer for 100BASE-TX mode (e.g. magnetics, termination, LPF)

Figure A.3 – General drawing of the circuit diagram for ESD tests of Ethernet transceivers in powered mode

The test circuit for powered ESD tests is similar to the test circuit for functional test except the coupling network and the ground plane connection point. For tests in powered mode the coupling port ESD1 IND is used.



Key

Components

A10	Ethernet transceiver 100BASE-T1 or 1000BASE-T1
C11	capacitor C = 4,7 nF (default value, placement depend on test case)
C12, C13, C22, C23	capacitor C = 100 nF
C41	capacitor C = 1 nF
C42	capacitor C = 330 pF
D11	diode, general purpose rectifier type
L11, L21	Common mode choke which satisfying the requirements in Annex E (placement depend on test case)
L41	inductor L = 47 µH
L42	impedance should be greater than 400 Ω in the frequency range of interest
R1, R2, R3, R4	resistor $R \geq$ 220 kΩ (placement is optional)
R11, R12	resistor R = 1 kΩ (± 1 % for 100BASE-T1, ± 0,5 % for 1000BASE-T1, default value, placement depend on test case)
R13	resistor R = 100 kΩ (default value, placement depend on test case)
R15	resistor R = 33 kΩ
X11, X12, X13, X14	Filter network or external circuitry defined by semiconductor manufacturer

Figure A.4 – General drawing of the circuit diagram for ESD tests of Ethernet transceivers in unpowered mode

The test circuit for unpowered ESD tests at Ethernet transceiver consists of a single Ethernet transceiver (A10) with external mandatory components (X11, X12, X13, X14), the BIN (L11, C12, C13, R11, R12, R13, C11) and a second BIN (L21, C22, C23) for connection to the Ethernet counterpart node. The value for the series resistor on the pin WAKE (R15) should be chosen according to the IC specification with minimum value (default R = 33 kΩ). All external mandatory components (except components for MDI) shall be used according to the specification of the Ethernet transceiver. If special components for MDI are defined in the specification, this circuitry should be tested in addition. The default parameters of the passive components in ESD coupling paths are for capacitors a tolerance of ±10 %, material X7R according to electronic industry association (see EIA-198-1) or similar, voltage rating ≥ 50 V and dimension 1206 or 0805. The default parameters for resistors are ±1 % tolerance and dimension 1206 or 0805. For tests in unpowered mode, the discharge points ESD1a, ESD1b, ESD2 and ESD3 and optional discharge resistors (R1, R2, R3, R4 with R ≥ 200 kΩ) will be used for ESD coupling. The second BIN (L21, C22, C23) is not connected during ESD test but is used to check the proper functionality of the transceiver after each single ESD test.

Annex B
(normative)

Test circuit boards

B.1 Test circuit board for transceiver network configuration

For functional conducted and powered ESD tests of Ethernet transceivers the test network shall be designed on a printed circuit board. To ensure good RF characteristics of transceiver with external circuitry and the coupling and decoupling networks, an equal design of the circuitry for node 1 and node 2 on a minimum four layer PCB with a GND layer is recommended.

A layout example for functional conducted tests is shown in Figure B.1.

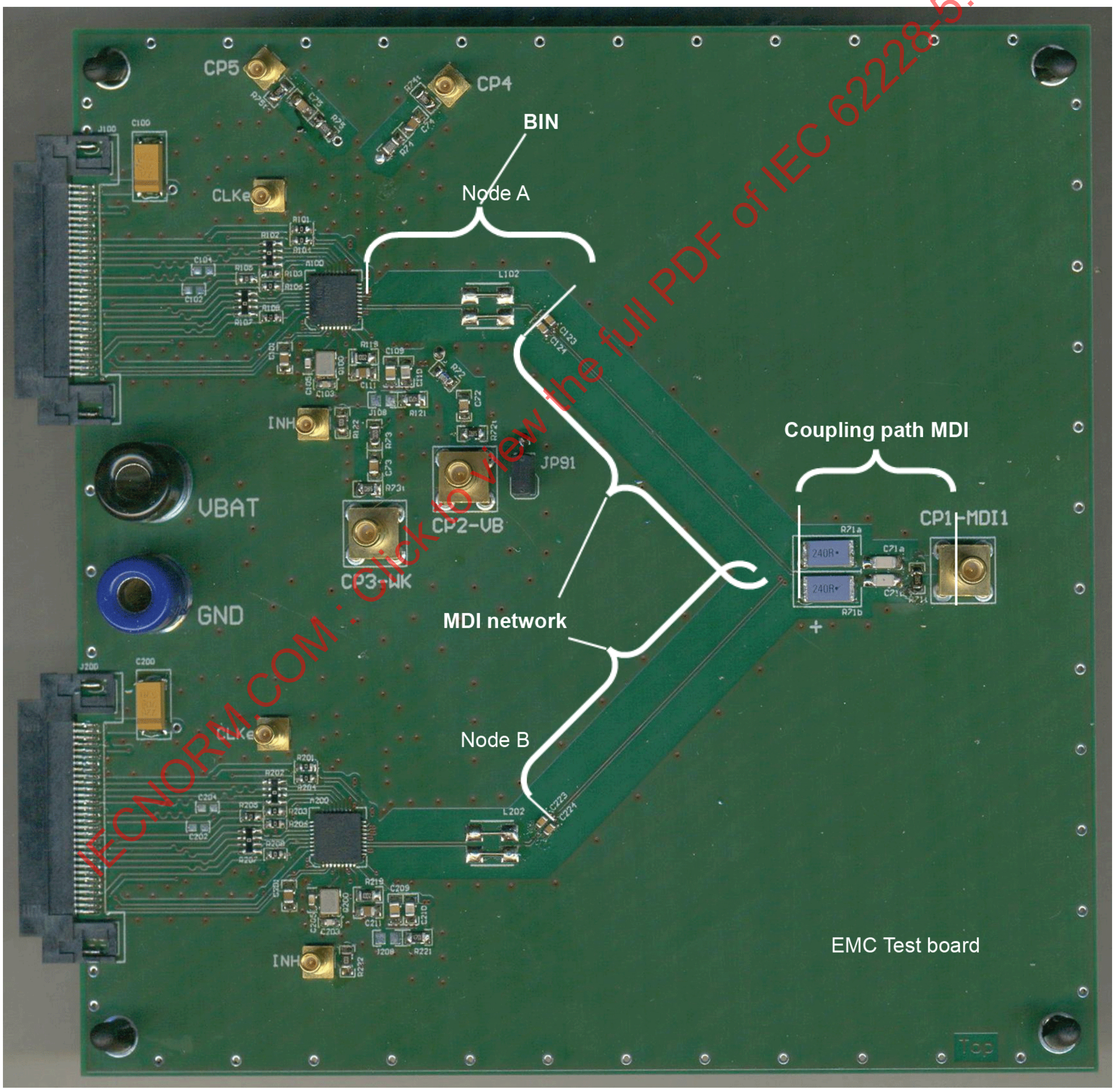
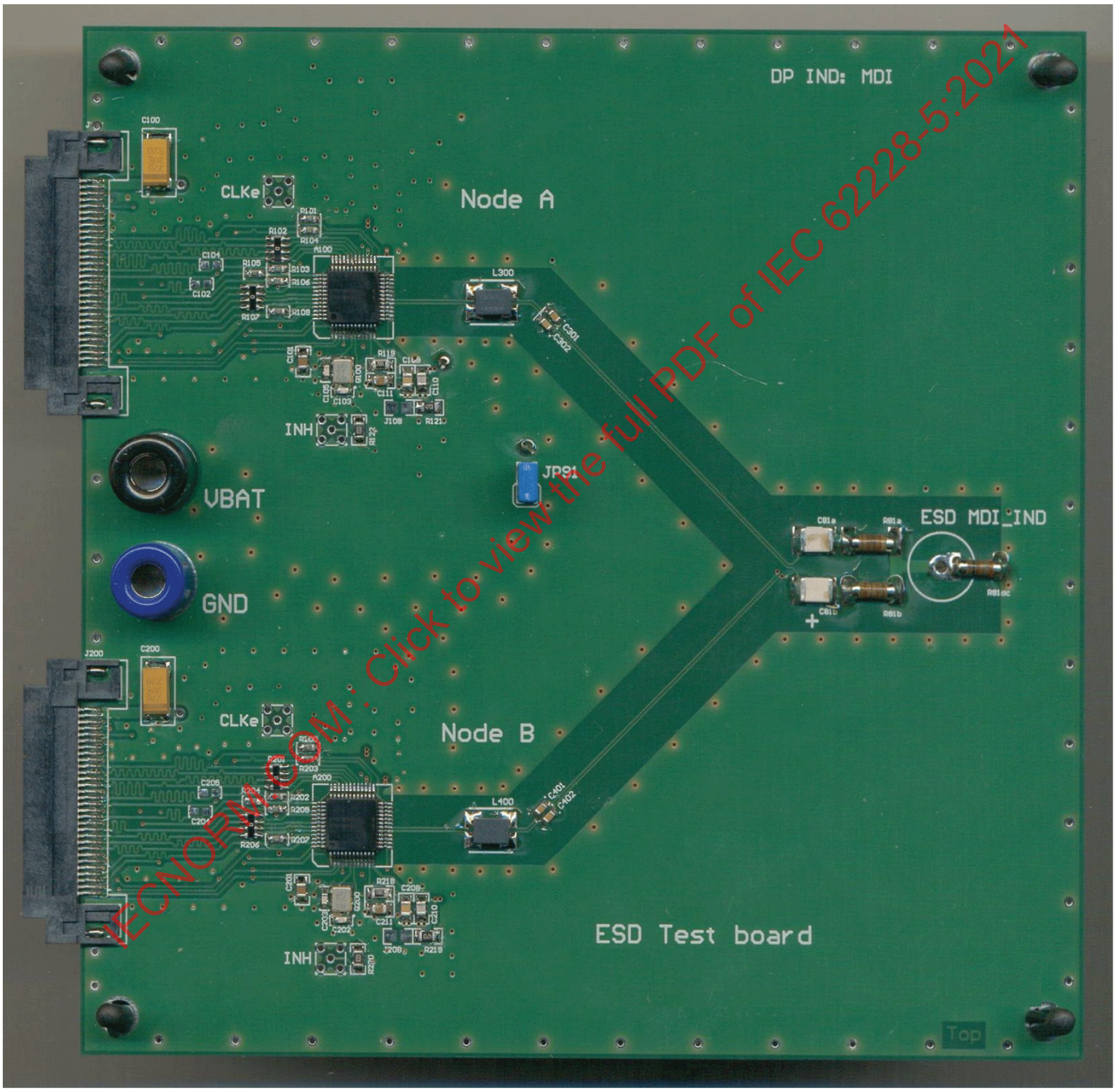


Figure B.1 – Example of functional conducted test board for Ethernet transceiver ICs (100BASE-T1)

The traces of MDI network between the BIN of node 1 and the BIN of node 2 (see Figure B.1) should have a length of 90 (± 10) mm with a differential line impedance of 100 (± 5) Ω. The length of the coupling paths on the test board should be kept as short as possible to ensure a parasitic inductance value of traces less than 5 nH. The DUT shall be soldered on the test board to minimize parasitic effects. For proper shielding, all connections from the test board to peripheral devices should be connected via coaxial printed circuit board sockets except for the filtered power supplies and GND.

A layout example for powered ESD tests is shown in Figure B.2. The pad for the discharge points ESD1 IMD shall be carried out in a way that a proper contact to the discharge tip of the test generator is ensured (e.g. by rounded vias in the layout of the ESD test board).



IEC

Figure B.2 – Example of powered ESD test board for Ethernet transceivers ICs (100BASE-T1)

B.2 Test circuit board for single transceiver configuration

For unpowered ESD tests, a printed circuit board shall be used. At least a four-layer construction of the PCB with GND layer is recommended. The pads for the discharge points ESD1a to ESD3 shall be carried out in a way that a proper contact to the discharge tip of the test generator is ensured (e.g. by rounded vias in the layout of the ESD test board). The discharge point shall be directly connected by a trace to the respective pin under test of the transceiver. The passive components of the network shall be placed close to the transceiver to reduce parasitic effects. The DUT should be soldered on the test board to ensure application like conditions and avoid parasitic setup effects by sockets. The insulation distance between the signal lines and pads of the passive components and the extensive ground area should be designed in a way that a spark over at these points can be prevented up to the intended test voltage level. A layout example is shown in Figure B.3 and Figure B.4.

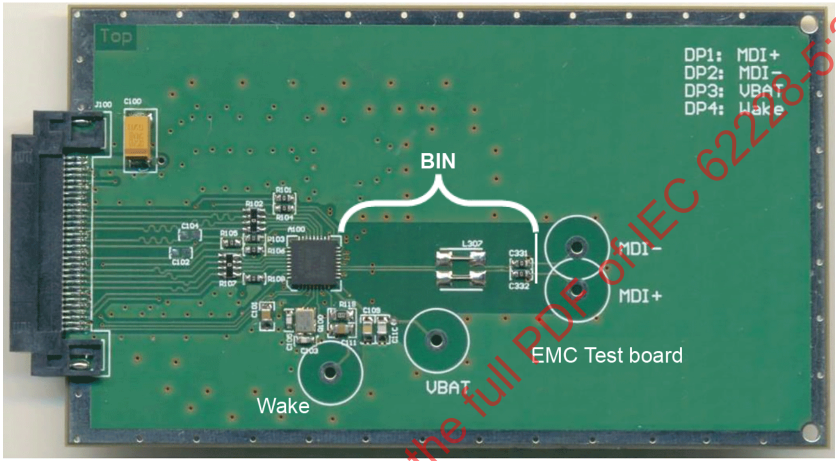


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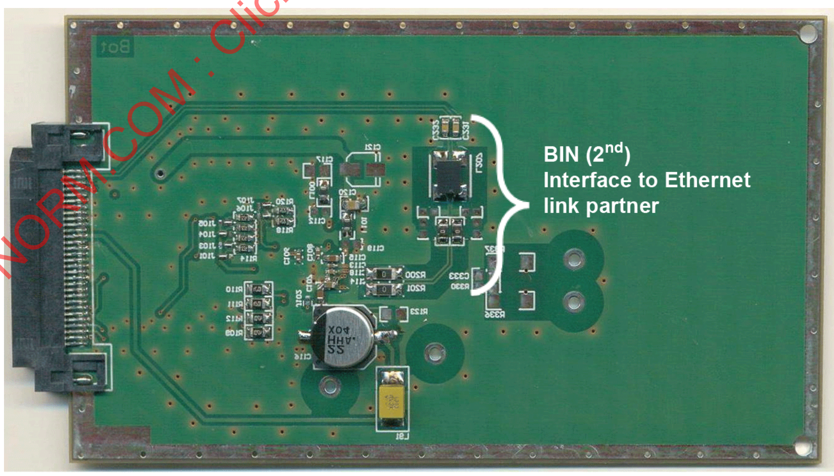
Figure B.3 – Example of unpowered ESD test board for Ethernet transceivers ICs (100BASE-T1), top layer



IEC

Figure B.4 – Example of unpowered ESD test board for Ethernet transceivers ICs (100BASE-T1), bottom layer

Further requirements for the ESD test board are defined in Table B.1.

Table B.1 – Parameter ESD test circuit board

Parameter	Value
Trace length between BIN and discharge point	15 (±5) mm
Trace width of the conducting path	0,254 mm

Annex C
(informative)

Test of Ethernet transceiver for radiated RF emission and RF immunity

C.1 General

This Annex C describes tests of Ethernet transceiver in regards to radiated disturbances. It contains definitions for test methods, test conditions, performance criteria, test procedures, test setups, test boards and recommended limits. The test methods covered by this annex include

- Radiated RF emission, and
- Radiated RF immunity.

C.2 General configuration for transceiver network

For evaluation of radiated RF emission and RF immunity characteristic of an Ethernet transceiver in functional operation mode, a minimal Ethernet test network consisting of one Ethernet transceiver (DUT) and an Ethernet link partner of the same type is used. The test configuration in general consists of Ethernet transceivers with external mandatory components (Ethernet node) in a minimal test network, where filtered power supplies, signals, monitoring probes and coupling networks are connected as shown in Figure C.1.

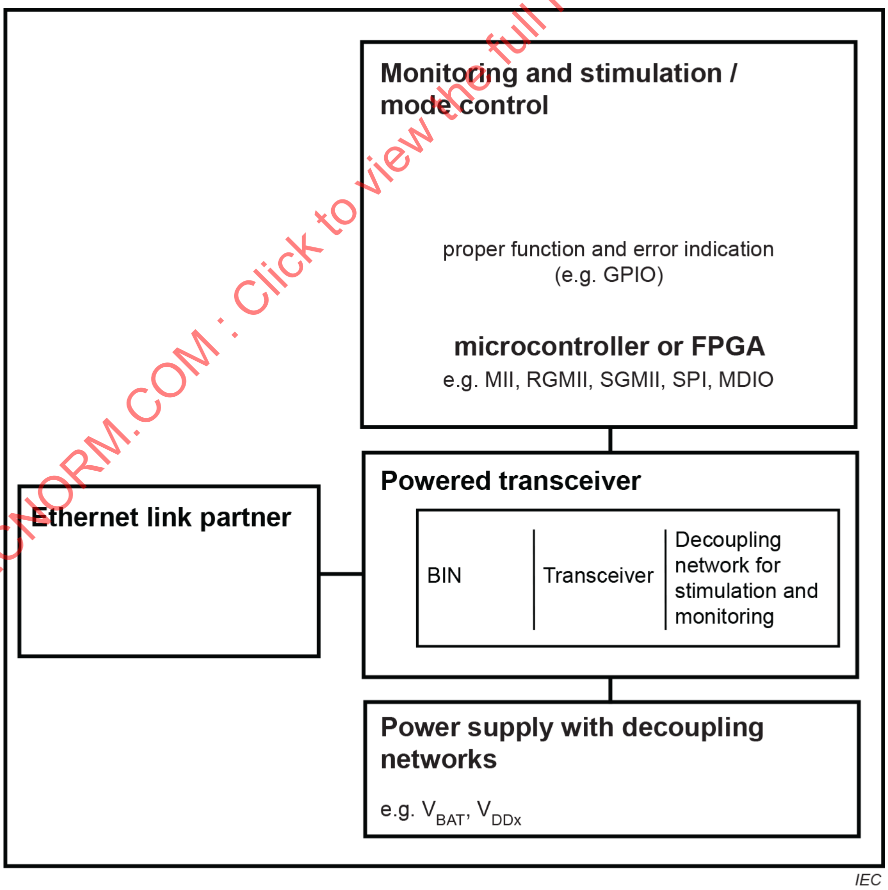


Figure C.1 – General test configuration for tests in transceiver network used for radiated tests

NOTE In specific cases, or for analyses a deviation from this setup can be agreed between the users of this document and will be noted in the test report.

The BIN configurations are described in 5.3. The DUT node is configured according to data sheet definitions of the semiconductor manufacturer to establish a full duplex Ethernet link with the Ethernet link partner. For the purpose of reproducibility of test results, the connection to the Ethernet link partner should have a length of (250 ± 20) mm and its characteristic should fulfill the definitions of the related Ethernet standard (ISO/IEC/IEEE 8802-3/AMD4 or ISO/IEC/IEEE 8802-3/AMD1 or ISO/IEC/IEEE 8802-3). Multiple external link partner connections of Ethernet switches with a higher number of MDI ports (e.g. 6 and more) could be limited because of test board constrains. In this case the Ethernet test links can be realized between different MDI ports of the switch itself but at least one port should be connected to an external link partner.

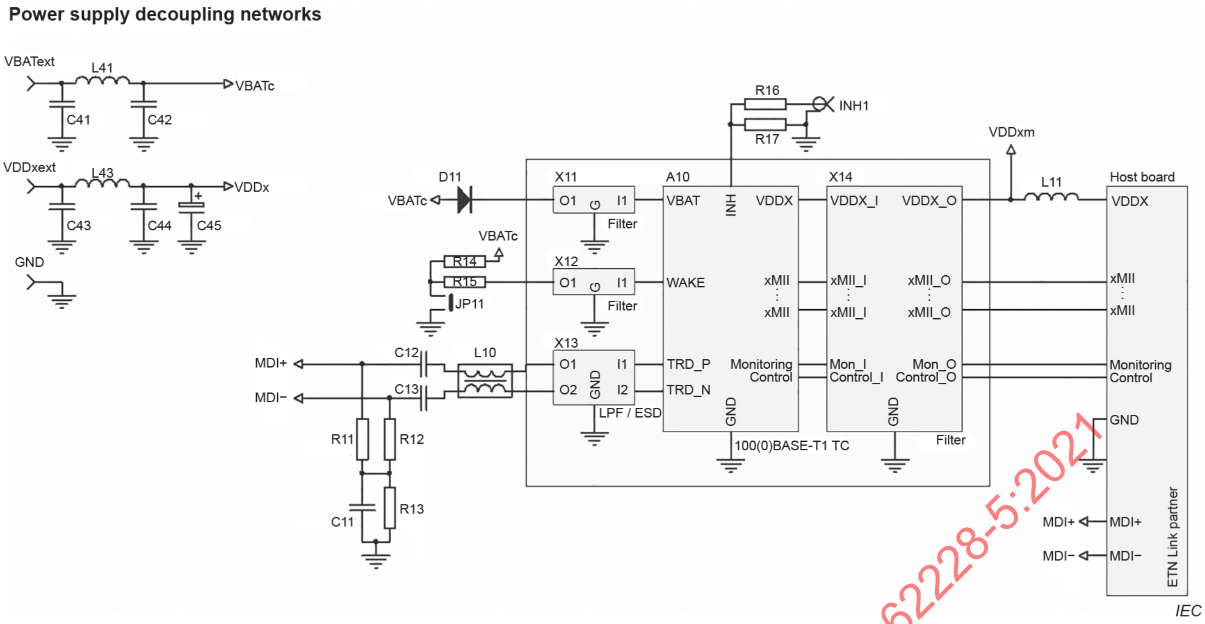
All available MII interfaces for the Ethernet transceiver (e.g. RGMII, SGMII) should be tested separately as described in 5.4.1.

C.3 Tests

C.3.1 General

The Ethernet test circuits for radiated RF tests define the details of the complete test circuitry for testing Ethernet transceivers in functional operating modes under network condition. It defines mandatory and optional components for Ethernet transceiver functions and components for coupling networks, decoupling networks which are used for power supply, stimulation and monitoring of the DUT.

A general drawing of the test circuit diagram of the Ethernet test network for testing 100BASE-T1 and 1000BASE-T1 Ethernet transceivers in functional operating modes for radiated RF tests is given in Figure C.2. The test circuit diagram for testing 100BASE-TX Ethernet transceivers should follow the definitions of Figure C.2 and Figure A.2.



Key
Components

A10	Ethernet transceiver 100BASE-T1 or 1000BASE-T1
C11	capacitor C = 4,7 nF (default value, placement depend on test case)
C12, C13	capacitor C = 100 nF
C41, C43	capacitor C = 1 nF
C42, C44	capacitor C = 330 pF
C45	capacitor C = 22 µF
D11	diode, general purpose rectifier type
JP11	Jumper
L10	Common mode choke which satisfying the requirements in Annex E (placement depend on test case)
L11	inductor L = 4,7 µH (only populated for emission measurements at V_{DDx})
L41	inductor L = 47 µH
R11, R12	resistor R = 1 kΩ (± 1 % for 100BASE-T1, ± 0,5 % for 1000BASE-T1, default value, placement depend on test case)
R13	resistor R = 100 kΩ (default value, placement depend on test case)
R14	resistor R = 3,3 kΩ
R15	resistor R = 33 kΩ
R16	resistor R = 1 kΩ
R17	resistor R = 10 kΩ
X11, X12, X13, X14	Filter network or external circuitry defined by semiconductor manufacturer

Figure C.2 – General drawing of the circuit diagram of test network for 100BASE-T1 and 1000BASE-T1 Ethernet transceivers for functional test using radiated RF test methods

A 100BASE-T1 and 1000BASE-T1 Ethernet node consists of transceiver (A10) with external mandatory components (X11, X12, X13, X14) and the BIN (L11, C12, C13, R11, R12, R13) and the decoupling network at monitored pins (R16).

All mandatory external components (except components for MDI) should be used according to the specification of the Ethernet transceiver. If special components for MDI are defined in the specification, this circuitry should be tested in addition.

The resistor values at the WAKE pin should be set to the maximum specified value (default R = 3,3 kΩ) for R14 and to the minimum specified value (default R = 33 kΩ) for R15.

For RF decoupling of monitored pins INH, the default resistor value is set to R = 1 kΩ for all tests.

In order to avoid a floating voltage at pin INH in sleep mode, a pull down resistor (R17) should be used with values according to the IC specifications (default R = 10 kΩ).

For decoupling of external power supplies two-stage LC-filters (C41, L41, C42 and C43, L43, C44, C45) are used separately for V_{BAT} and V_{DDx}.

For radiated tests of Ethernet transceivers the test network should be designed on a printed circuit board that is different to the test board for conducted RF and transient tests and follows the definitions of IEC 61967-1 and IEC 62132-1.

An example for radiated RF test board is given in Figure C.3 and Figure C.4.

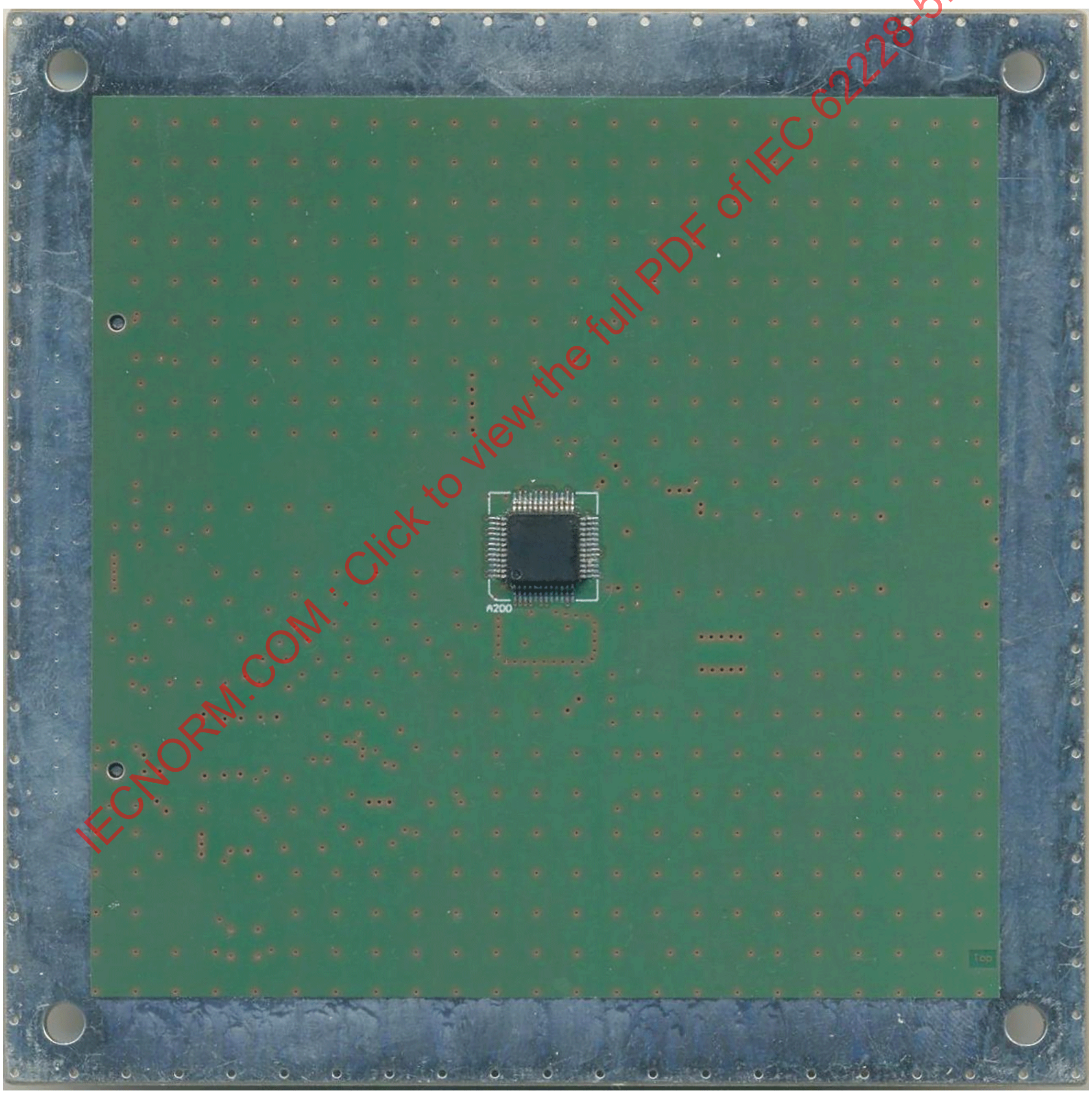
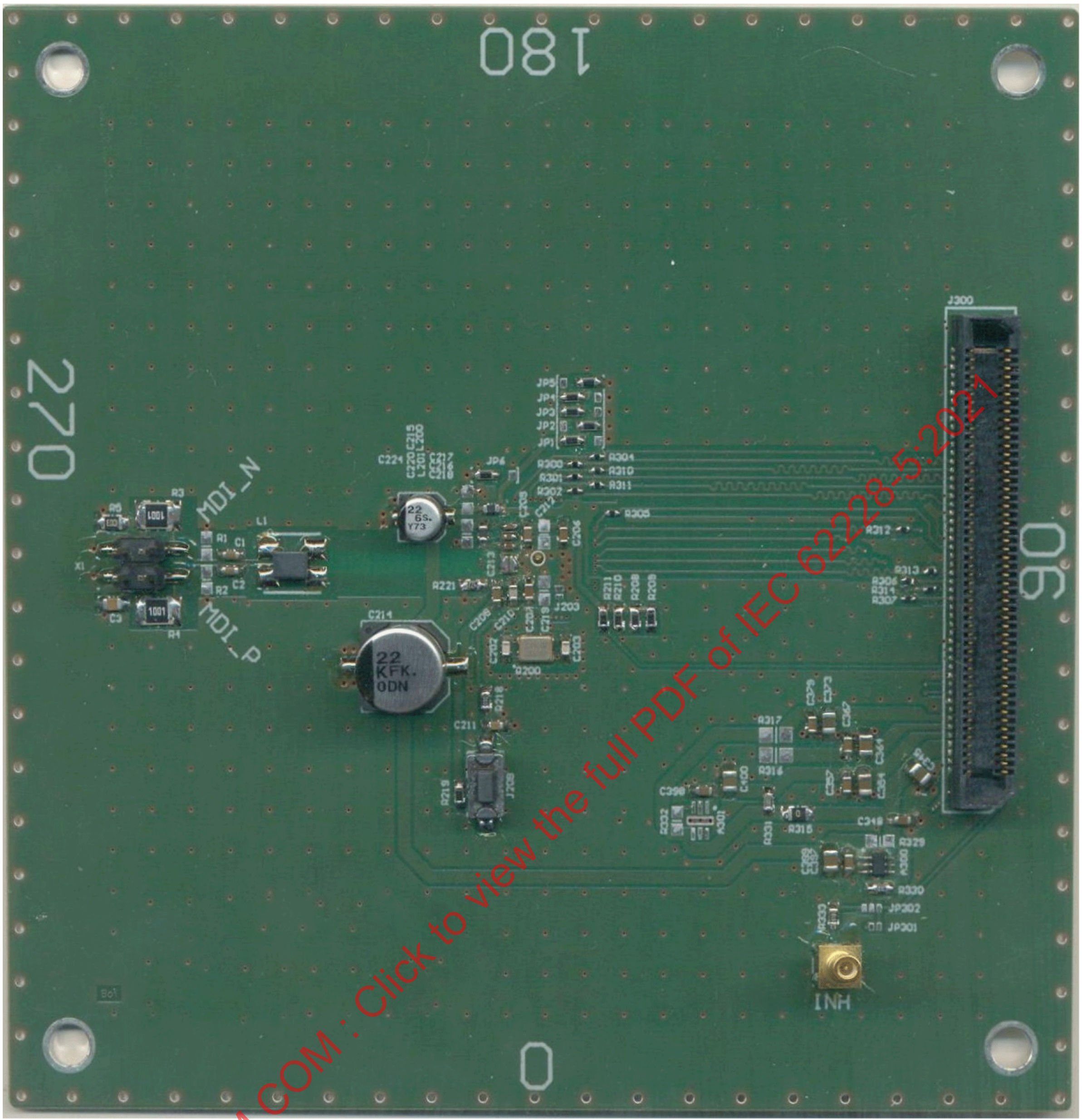


Figure C.3 – Example of functional radiated test board for Ethernet transceiver ICs (100BASE-T1), top layer (DUT side)



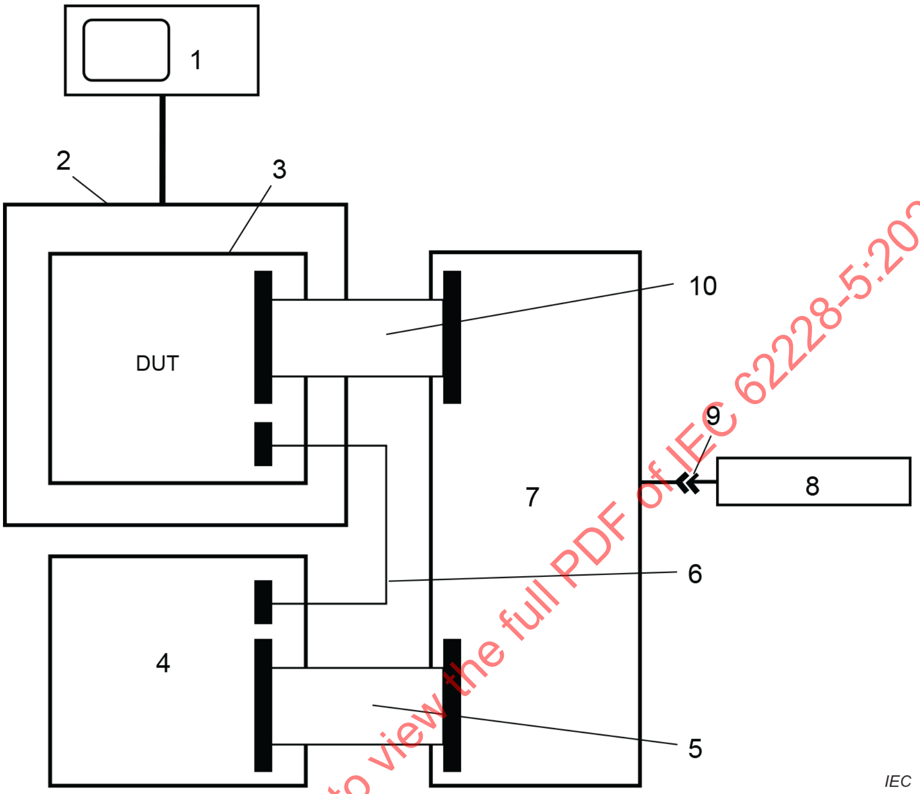
IEC

Figure C.4 – Example of functional radiated test board for Ethernet transceiver ICs (100BASE-T1), bottom layer (external circuitry side)

C.3.2 Emission of radiated RF disturbances

The measurement of the radiated RF emission should be performed by IC stripline method according to IEC 61967-8 or by GTEM cell method according to IEC 61967-2.

The test setup for radiated RF emission measurement of transceiver is shown in Figure C.5.



Key

1	Spectrum analyzer / EMI receiver	6	MDI interface
2	IC stripline or GTEM cell	7	Controller board
3	Test board	8	Power supply (V_{BAText}, V_{DDx_ext}, GND)
4	Ethernet link partner	9	Connector
5	Interface to link partner	10	Controller interface

Figure C.5 – Test setup for measurement of radiated RF emission

The test equipment definitions are the following:

- spectrum analyzer / EMI receiver;
- IC stripline including 50 Ω RF termination resistor for output or GTEM cell;
- test board for radiated RF tests;
- controller board;
- board with Ethernet link partner (test board as used for conducted RF emission, DPI and transient tests is proposed), and
- power supply.

The settings of the radiated RF measurement equipment are given in Table C.1.

Table C.1 – Settings of the radiated RF measurement equipment

RF Measurement equipment	Spectrum analyzer	EMI receiver
Detector	Peak	
Frequency range	0,15 MHz to 3000 MHz (6000 MHz optional)	
Resolution bandwidth (RBW) 150 kHz to 30 MHz: 30 MHz to 6000 MHz:	 10 kHz 100 kHz	 9 kHz 120 kHz
Video bandwidth (VBW)	≥ 3 times RBW	–
Numbers of sweeps	10 (max hold)	–
Measurement time per step	–	≥ 100 ms
Frequency sweep time	≥ 4 000 s	–
Frequency step width 150 kHz to 30 MHz: 30 MHz to 6000 MHz:	 – –	 ≤ 5 kHz ≤ 50 kHz
FFT based EMI receivers can be used as well if they meet CISPR 16-1-1 definitions.		

The radiated RF emission measurements should be performed according to Table C.2.

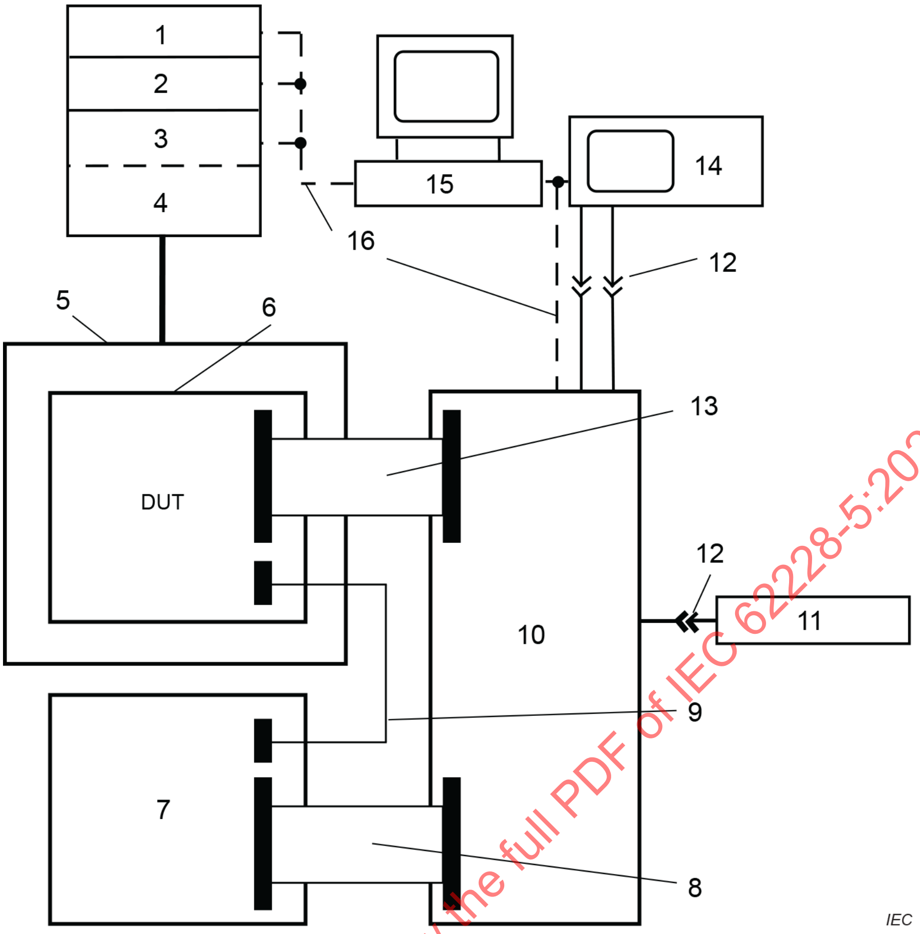
Table C.2 – Radiated RF emission measurements

Transceiver mode	DUT orientation [a]	MDI test network (BIN)	Ethernet system		
			1000BASE-T1	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	0°, 90°	Opt-BIN	X	X	X
X A test should be performed.					
[a] DUT orientation within IC stripline or GTEM cell					

C.3.3 Immunity to radiated RF disturbances

The test of the radiated RF immunity should be performed by IC Stripline method according to IEC 62132-8 or by GTEM cell method according to IEC 62132-2.

The test setup for radiated RF immunity tests of transceiver is shown in Figure C.6.



Key

1	RF generator	9	MDI interface
2	RF amplifier	10	Controller board
3	RF power meter	11	Power supply (V_{BAText}, V_{DDx_ext}, GND)
4	Directional coupler	12	Connector
5	IC stripline or GTEM cell	13	Controller interface
6	Test board	14	DSO (optional)
7	Ethernet link partner	15	Control PC (optional)
8	Interface to link partner	16	Remote control (optional)

Figure C.6 – Test setup for radiated RF immunity tests

The test equipment definitions are the following:

- RF generator;
- RF amplifier;
- power meter with directional coupler;
- IC Stripline including 50 Ω RF termination resistor for output or GTEM cell;
- test board for radiated RF tests;
- controller board;
- board with Ethernet link partner (test board as used for conducted RF emission, DPI and transient tests is proposed);
- power supply;

- control PC (optional);
- digital storage oscilloscope (DSO, optional).

To determine the radiated RF immunity of the Ethernet transceiver, tests with the parameters given in Table C.3 should be carried out.

Table C.3 – Specifications for radiated RF immunity tests

Item	Parameter	
Frequency	Range	Step
	1 MHz to 10 MHz	0,25 MHz
	10 MHz to 100 MHz	1 MHz
	100 MHz to 200 MHz	2 MHz
	200 MHz to 400 MHz	4 MHz
	400 MHz to 3 000 MHz	10 MHz
	3 000 MHz to 6 000 MHz (optional)	20 MHz
Minimum test field strength	50 V/m	
Maximum field strength	800 V/m	
Field strength step size	50 V/m	
Dwell time	1 s	
Modulation (including optional frequency ranges)	f = 1 MHz to 6 000 MHz: CW f = 1 MHz to 800 MHz: AM 80 % 1 kHz ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 806 MHz to 915 MHz: PM 217 Hz, ton 577 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 1200 MHz to 1 400 MHz: PM 300 Hz, ton 3 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 1710 MHz to 1 910 MHz: PM 217 Hz, ton 577 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 2700 MHz to 3 400 MHz: PM 300 Hz, ton 3 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) f = 3 400 MHz to 6 000 MHz: PM 1600 Hz, ton 312,5 µs ($\hat{P}_{PM} = \hat{P}_{CW}$)	
Test procedure for evaluation of functional status class A_{IC}	Searching for malfunction during the complete dwell time while test field strength is stepwise increased. An optimized control procedure can be used to reduce the test time but ensuring that there are no artifacts in DUT response during frequency or test field strength steps. EXAMPLE: Procedure for each frequency step: – start with maximum test value or with the level that caused a malfunction at the previous frequency step, – in case of malfunction at this test level reduce the test value by 6dB and repeat the test, – increase the test value stepwise until a malfunction occurs or the maximum field strength is reached, – the immunity level at this frequency is the maximum field strength that causes no malfunction.	

The tests for functional status class A_{IC} evaluation should be performed according to Table C.4. For each test, an immunity threshold curve with the field strength as the parameter should be determined and documented in a diagram in the test report.

Table C.4 – Radiated RF immunity tests for functional status class AIC evaluation of Ethernet transceivers

Transceiver mode	DUT orientation [a]	MDI test network (BIN)	Failure validation for error / function					
			CRC, Link, DTT	SNR or SQI	RS-FEC	Sum [b]	Other pin function	Wake-up
Ethernet system			1000BASE-T1 / 100BASE-T1 / 100BASE-TX					
normal mode / Ethernet test communi-cation	0°, 90°	Opt-BIN				X/X/X	X/X/X	

X A test should be performed.

[a] DUT orientation within IC stripline or GTEM cell

[b] Sum error: Link, CRC, and DTT or Link and BIST / PRBS tests status evaluated in parallel.

Annex D
(informative)

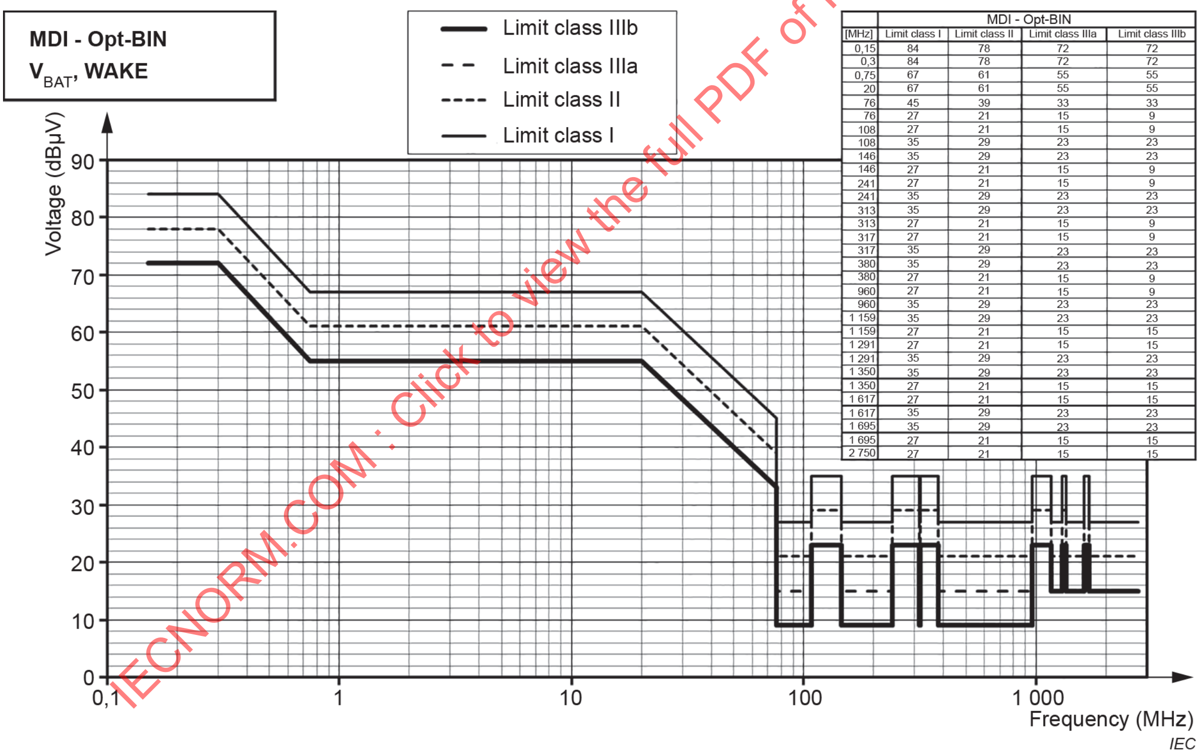
Examples for test limits for Ethernet transceiver in automotive application

D.1 General

The purpose of this Annex D is to show examples of limits for Ethernet transceivers used in automotive applications. Because of possible different cable implementation for 1000BASE-T1 using unshielded twisted pair (UTP) or shielded twisted pair (STP), different limits are given. For specific limit selection, refer to the applicable test method documents.

D.2 Emission of conducted RF disturbances

Figure D.1 and Figure D.2 give an example of limits for conducted RF emission measurements at the pins MDI (using Opt-BIN), V_{BAT}, WAKE and V_{DDX} for the 150 Ω direct coupling method according to IEC 61967-4. Test cases with recommended limit classes are given in Table D.1.



	MDI - Opt-BIN			
[MHz]	Limit class I	Limit class II	Limit class IIIa	Limit class IIIb
0,15	84	78	72	72
0,3	84	78	72	72
0,75	67	61	55	55
20	67	61	55	55
76	45	39	33	33
76	27	21	15	9
108	27	21	15	9
108	35	29	23	23
146	35	29	23	23
146	27	21	15	9
241	27	21	15	9
241	35	29	23	23
313	35	29	23	23
313	27	21	15	9
317	27	21	15	9
317	35	29	23	23
380	35	29	23	23
380	27	21	15	9
960	27	21	15	9
960	35	29	23	23
1 159	35	29	23	23
1 159	27	21	15	15
1 291	27	21	15	15
1 291	35	29	23	23
1 350	35	29	23	23
1 350	27	21	15	15
1 617	27	21	15	15
1 617	35	29	23	23
1 695	35	29	23	23
1 695	27	21	15	15
2 750	27	21	15	15

Figure D.1 – Example of limits for conducted RF emission – MDI Opt-BIN, V_{BAT} and WAKE

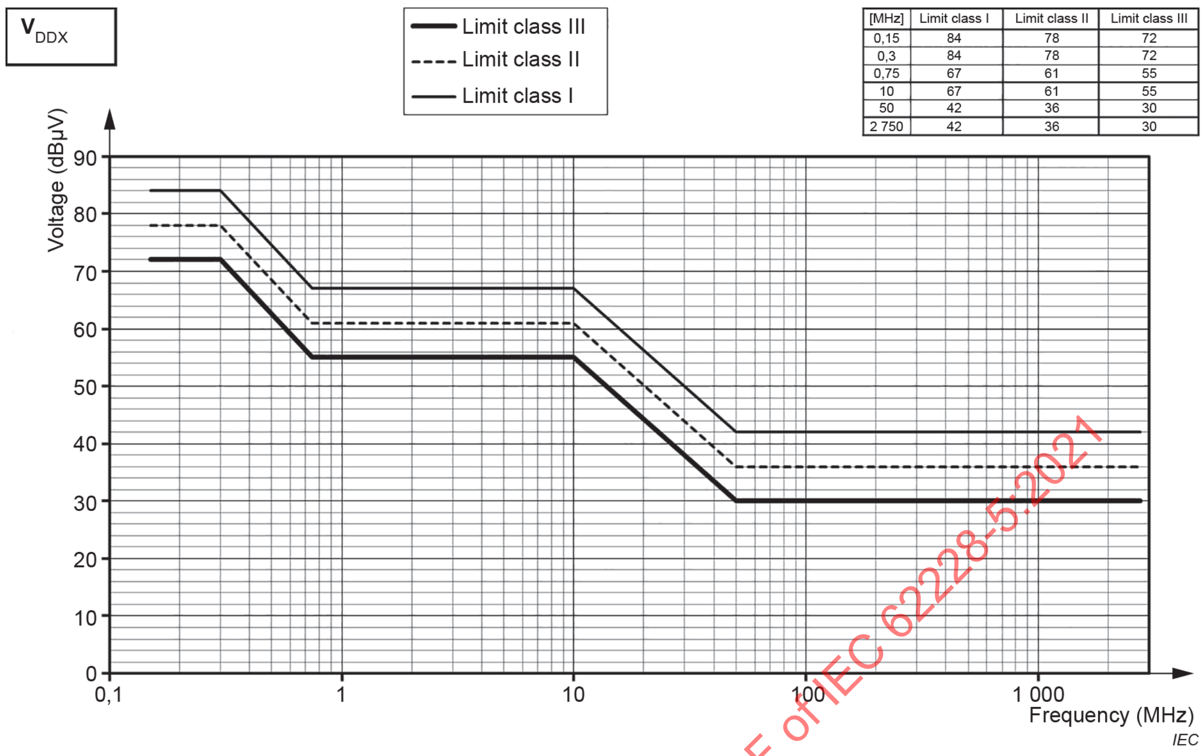


Figure D.2 – Example of limits for conducted RF emission – local supplies

Table D.1 – Example of limits for conducted RF emission – test cases with recommended limit classes

Transceiver mode	Coupling port	Pin	MDI test network (BIN)	Ethernet system			
				1000BASE-T1 UTP [a]	1000BASE-T1 STP [b]	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	EMI1 (symmetric)	MDI	Opt-BIN	specific requirement / to be defined by system implementer	Class I	Class IIIb	Class I
	EMI1a,b (1,25% unbalance)		Opt-BIN		Class I	-	-
	EMI1c,d (2,5% unbalance)		Opt-BIN	-		Class IIIb	Class I
	EMI2	V_{BAT}	Opt-BIN	Class IIIb		Class IIIb	Class IIIb
	EMI3	WAKE	Opt-BIN	Class IIIb		Class IIIb	Class IIIb
	EMI4	V_{DDx}	Opt-BIN	Class III		Class III	Class III

[a] For 1000BASE-T1 systems using unshielded twisted pair (UTP) cables.

[b] For 1000BASE-T1 systems using shielded twisted pair (STP) cables.

D.3 Immunity to conducted RF disturbances

Figure D.3, Figure D.4, Figure D.5 and Figure D.6 give an example of limits for conducted RF immunity tests at the pins MDI (using Opt-BIN), V_{BAT} and WAKE for the DPI test method according to IEC 62132-4. There are different target levels for functional tests related to functional status class A_{IC} and functional status class C_{IC} or D_{IC}. Test cases with recommended limit classes are given in Table D.2and Table D.3.

MDI - Opt-BIN

[MHz]	Limit class I (A_IC)	Limit class II (A_IC)	Limit class III (A_IC)	Limit class IV (A_IC)
1	12	15	18	21
8	30	33	36	39
88	30	33	36	39
1 000	24	27	30	33
2 000	22,25	25,25	28,25	31,25

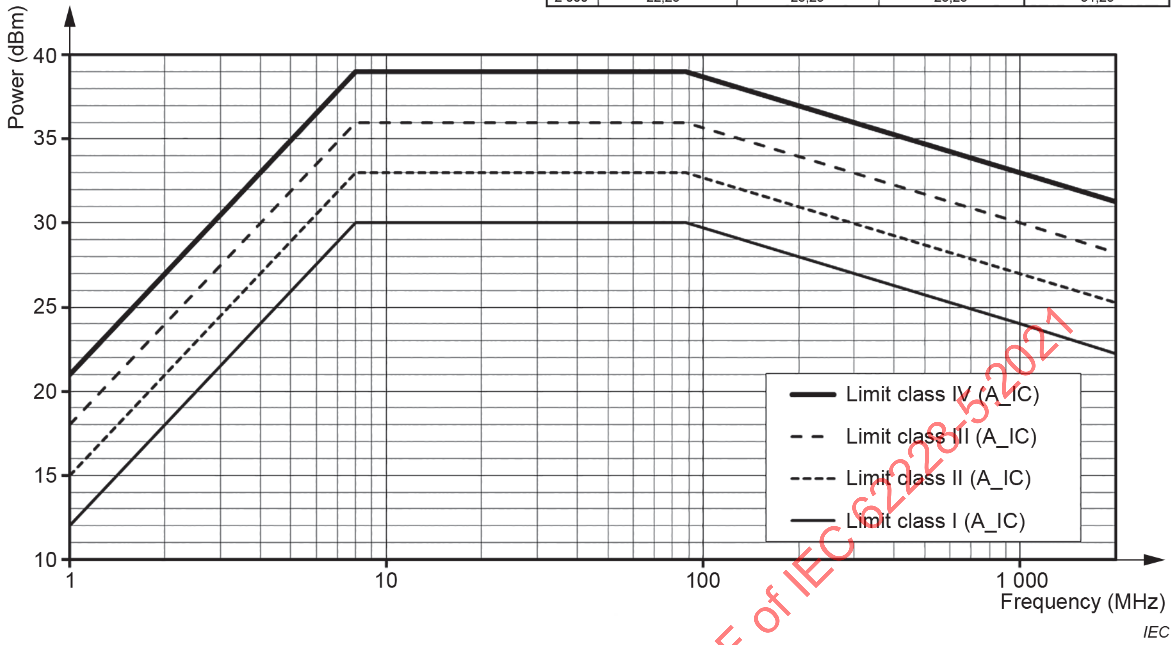


Figure D.3 – Example of limits for conducted RF immunity for functional status class A_{IC} – MDI Opt-BIN

V_{BAT} WAKE

[MHz]	Limit class I (A_IC)	Limit class II (A_IC)	Limit class III (A_IC)
1	9	12	15
8	27	30	33
88	27	30	33
1 000	21	24	27

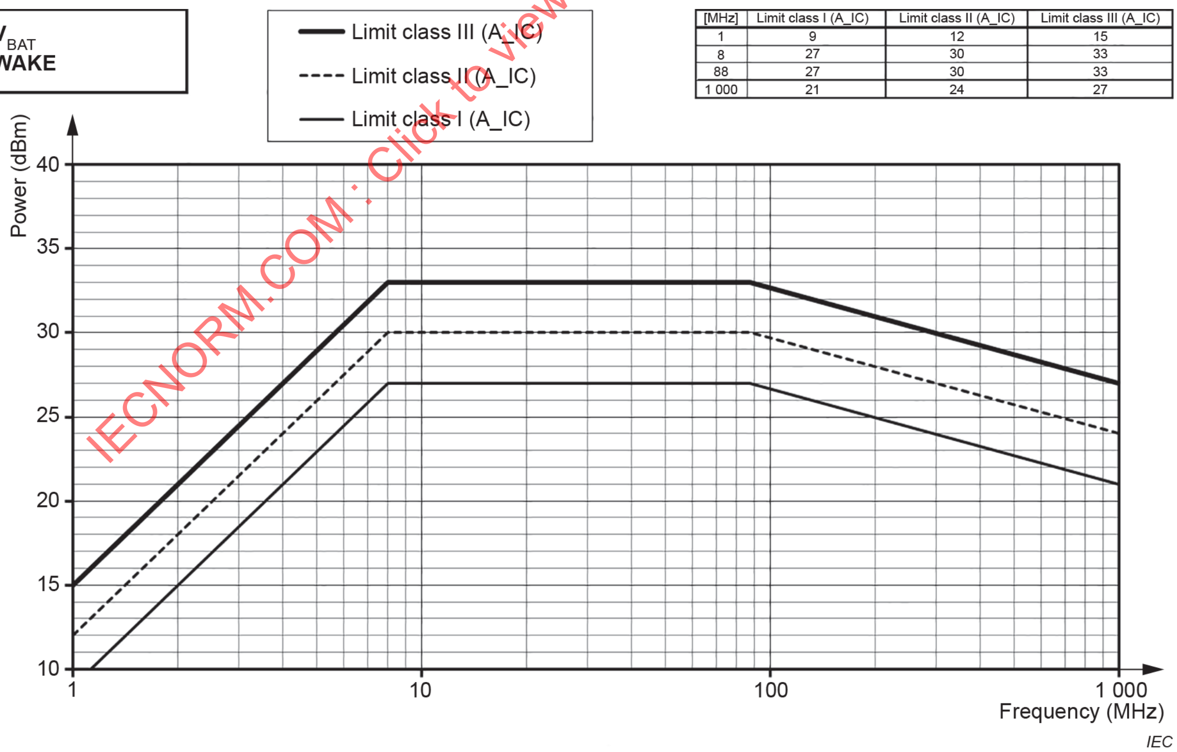


Figure D.4 – Example of limits for conducted RF immunity for functional status class A_{IC} – V_{BAT} and WAKE

Table D.2 – Example of limits for conducted RF immunity – test cases with recommended limit classes for functional status class A_{IC}

Transceiver mode	Coupling port	Pin	MDI test network (BIN)	Ethernet system			
				1000BASE-T1 UTP [a]	1000BASE-T1 STP [b]	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	RF1 (symmetric)	MDI	Opt-BIN	Class IV	Class I	Class IV	Class I
	RF1a,b (1,25% unbalance)		Opt-BIN	Class IV	Class I	-	-
	RF1c,d (2,5% unbalance)		Opt-BIN	-		Class IV	Class I
	RF2	V_{BAT}	Opt-BIN	Class III		Class III	Class I
	RF3	WAKE	Opt-BIN	Class III		Class III	Class I
low power mode / test of unwanted wakeup	RF1 (symmetric)	MDI	Opt-BIN	Class IV	Class I	Class IV	Class I
	RF1a,b (1,25% unbalance)		Opt-BIN	Class IV	Class I	-	-
	RF1c,d (2,5% unbalance)		Opt-BIN	-		Class IV	Class I
	RF2	V_{BAT}	Opt-BIN	Class III		Class III	Class III
	RF3	WAKE	Opt-BIN	Class III		Class III	Class III
low power mode / test of wanted wakeup	RF1 (symmetric)	MDI	Opt-BIN	Class IV	Class I	Class IV	Class I
	RF1a,b (1,25% unbalance)		Opt-BIN	Class IV	Class I	-	-
	RF1c,d (2,5% unbalance)		Opt-BIN	-		Class IV	Class I

[a] For 1000BASE-T1 systems using unshielded twisted pair (UTP) cables.

[b] For 1000BASE-T1 systems using shielded twisted pair (STP) cables.

MDI - Opt-BIN

[MHz]	Limit class I (C_IC/D_IC)	Limit class II (C_IC/D_IC)	Limit class III (C_IC/D_IC)	Limit class IV (C_IC/D_IC)
1	12	15	18	21
8	30	33	36	39
88	30	33	36	39
1 000	24	27	30	33
2 000	22,25	25,25	28,25	31,25

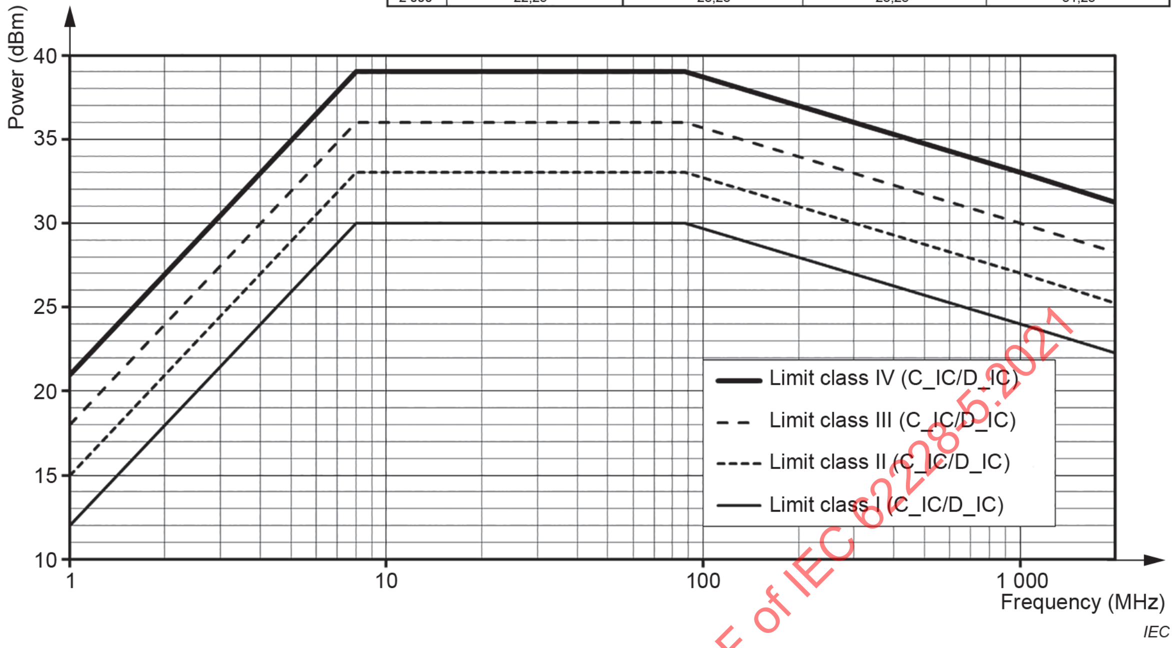


Figure D.5 – Example of limits for conducted RF immunity for functional status class C_{IC} or D_{IC} – MDI Opt-BIN

V_{BAT} WAKE

[MHz]	Limit class I (C_IC/D_IC)	Limit class II (C_IC/D_IC)	Limit class III (C_IC/D_IC)
1	12	15	18
8	30	33	36
88	30	33	36
1 000	24	27	30

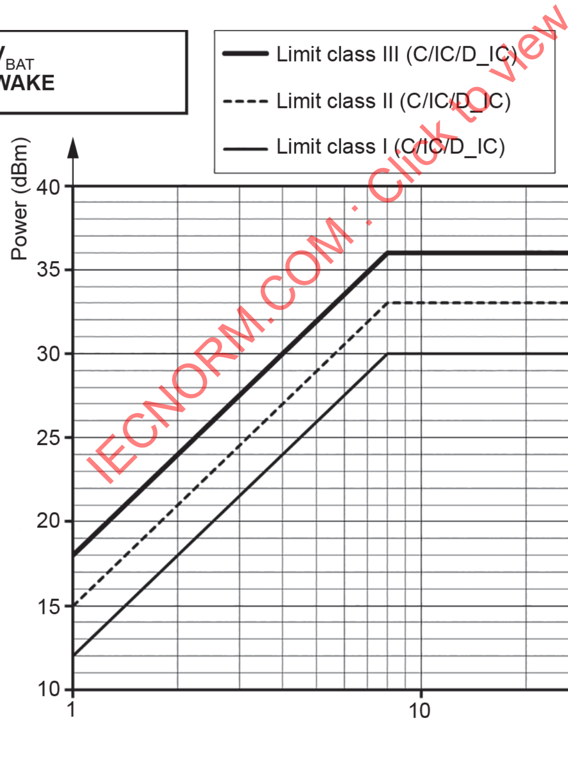


Figure D.6 – Example of limits for conducted RF immunity for functional status class C_{IC} or D_{IC} – V_{BAT} and WAKE

Table D.3 – Example of limits for conducted RF immunity – test cases with recommended limit classes for functional status class C_{IC} or D_{IC}

Transceiver mode	Coupling port	Pin	MDI test network (BIN)	Ethernet system			
				1000BASE-T1 UTP [a]	1000BASE-T1 STP [b]	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	RF1 (symmetric)	MDI	Opt-BIN	Class IV	Class I	Class IV	Class IV
	RF2	V_{BAT}	Opt-BIN	Class III		Class III	Class III
	RF3	WAKE	Opt-BIN	Class III		Class III	Class III

[a] For 1000BASE-T1 systems using unshielded twisted pair (UTP) cables.

[b] For 1000BASE-T1 systems using shielded twisted pair (STP) cables.

D.4 Immunity to impulses

Table D.4 gives an example of limits for impulse immunity tests at the pins MDI (Opt-BIN), V_{BAT} and WAKE using the non-synchronous transient injection method according to IEC 62215-3. Test cases with recommended limit classes are given in Table D.5.

Table D.4 – Example of limits for impulse immunity – Class I

Test pulse	V_{smax} V
1	− 100
2a	+ 75
3a	− 150
3b	+ 100

Table D.5 – Example of limits for impulse immunity – test cases with recommended limit classes for functional status class C_{IC} or D_{IC}

Transceiver mode	Coupling port	Pin	MDI test network (BIN)	Ethernet system		
				1000BASE-T1	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	IMP1	MDI	Opt-BIN	Class I	Class I	Class I
	IMP2	V_{BAT}	Opt-BIN	Class I	Class I	Class I
	IMP3	WAKE	Opt-BIN	Class I	Class I	Class I

D.5 Electrostatic discharge (ESD)

Table D.6 gives an example of limits for powered and unpowered ESD tests defined for functional status class A_{IC}, C_{IC} or D_{IC} evaluation at the pins MDI (Opt-BIN), V_{BAT} and WAKE.

Table D.6 – Example of limits for powered and unpowered ESD tests – test cases with recommended limits for functional status class $A1_{IC}$, $A2_{IC}$, $A3_{IC}$, C_{IC} or D_{IC}

Transceiver mode	Coupling port	Pin	MDI test network (BIN)	Failure validation for status class				
				$A1_{IC}$ (Link error)	$A2_{IC}$ (CRC, DTT error)	$A3_{IC}$ (unwanted wake up)	C_{IC}	D_{IC} (Damage)
Ethernet system				1000BASE-T1 / 100BASE-T1 / 100BASE-TX				
Powered / Test sequence from low power mode to normal mode	ESD1 IND	MDI	Opt-BIN	3 kV	-	3 kV	3 kV	6 kV
Unpowered	ESD1a, ESD1b	MDI	Opt-BIN	-				6 kV
	ESD2	V_{BAT}	Opt-BIN					6 kV
	ESD3	WAKE	Opt-BIN					6 kV

D.6 Emission of radiated RF disturbances

Examples of limits for radiated RF emission measurements using a 6,7 mm IC stripline according to IEC 61967-8 are given in Figure D.7. Test cases with recommended limit classes are given in Table D.7.

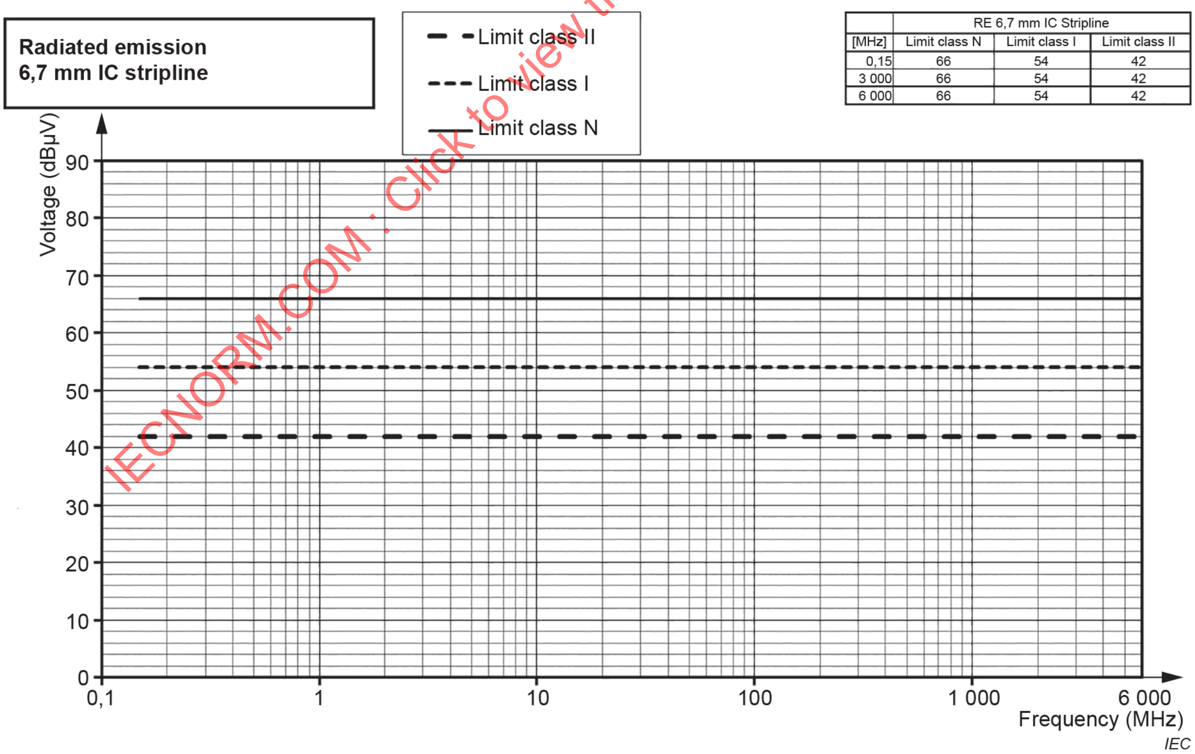


Figure D.7 – Example of limits for radiated RF emission for IC stripline with 6,7 mm active conductor height

A conversion factor (X) to correlate measuring results of IC striplines with different heights or GTEM cells to the default IC stripline height of 6,7 mm (IEC 61967-8) can be calculated by:

$$X = 20 \times \log \frac{h_1}{h_2}$$

where

X = conversion factor (in dB) to IC stripline 6,7 mm height type results;

h_1 = active conductor height (in mm) of specific IC stripline type or GTEM cell;

h_2 = active conductor height of 6,7 mm type.

Table D.7 – Example of limits for radiated RF emission – test cases with recommended limit classes

Transceiver mode	MDI test network (BIN)	Ethernet system		
		1000BASE-T1	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	Opt-BIN	Class II	Class II	Class II

D.7 Immunity to radiated RF disturbances

Figure D.8 gives an example of limits for radiated RF immunity tests. Test cases with recommended limit classes are given in Table D.8.

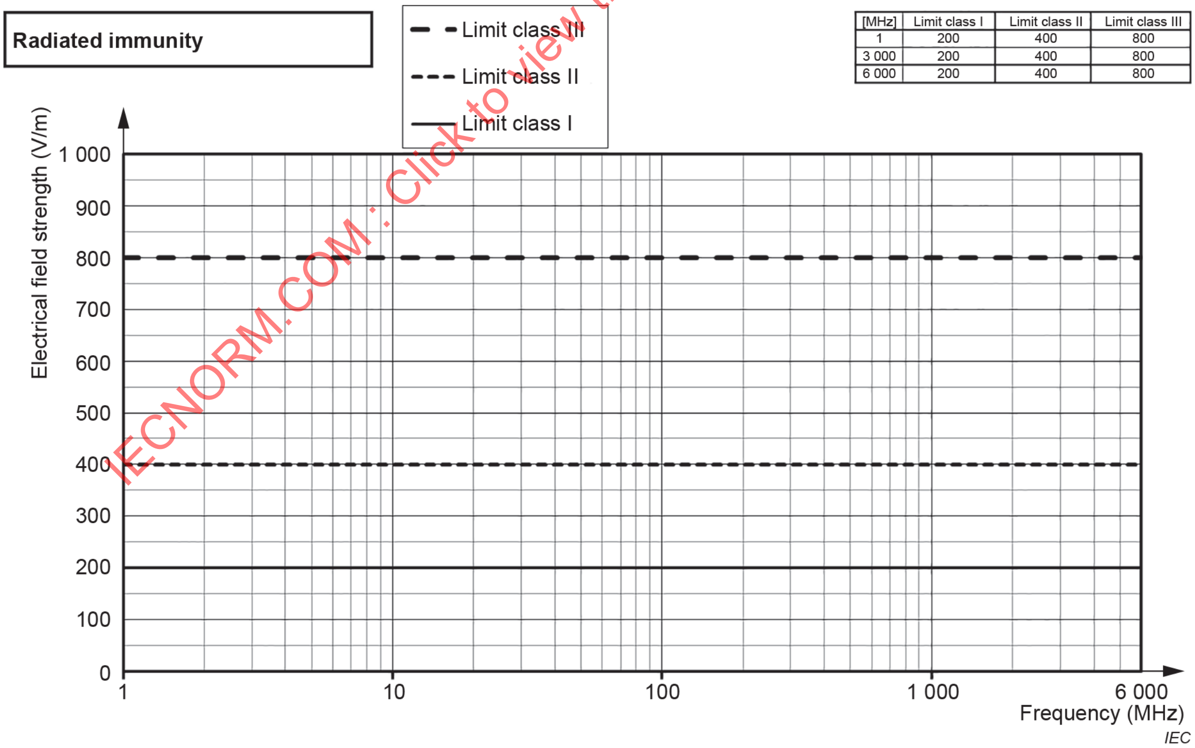


Figure D.8 – Example of limits for radiated RF immunity

Table D.8 – Example of limits for radiated RF immunity – test cases with recommended limit classes

Transceiver mode	MDI test network (BIN)	Ethernet system		
		1000BASE-T1	100BASE-T1	100BASE-TX
normal mode / with Ethernet test communication	Opt-BIN	Class II	Class II	Class II

Annex E
(informative)

Characterization of common mode chokes for EMC evaluation of Ethernet transceivers

E.1 General

Common mode chokes can have a significant effect on EMC test results in communication networks due to e.g. core saturation, differential mode impedance mismatch and asymmetric winding. To get comparable and reliable results for EMC evaluation of Ethernet transceivers, the characteristics of the used common mode chokes should be known and verified.

In this Annex E, test procedures for the characterization of CMCs intended to be used for Ethernet interfaces for 100BASE-T1 and 1000BASE-T1 are described. It contains definitions for test methods, test conditions, performance criteria, test procedures, test setups, test boards and recommended limits. The test methods covered by this annex include

- S-parameter measurement mixed mode;
- ESD damage test;
- saturation test at RF disturbances;
- saturation test at ESD;
- TDR measurement of differential mode impedance.

This annex does not cover devices that are intended for use in ISO/IEC/IEEE 8802-3:2017/AMD8 power over data line applications.

E.2 Test

E.2.1 General

In general, a printed circuit board with RF board-to-coax connectors should be used for all tests. To ensure reliable RF parameters, a test board with at least two layers with enlarged GND reference plane is required. The traces on the test board should be designed as 50 (± 5) Ω single ended transmission lines with a length as short as possible. For design of CMC footprint and the definition of minimal distance of CMC housing and CMC terminals to the GND plane the related specification of CMC manufacturer should be used, if not otherwise specified in the specific tests.

The test board design and the method of connecting the CMC with the test board is intended to provide high accuracy and reproducible test results and is with more details described in the respective measurement chapters.

A general electrical drawing with winding and pin definitions of a CMC is shown in Figure E.1.

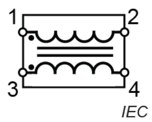
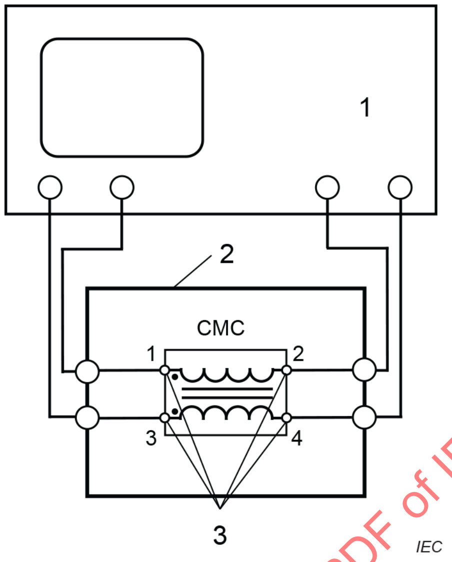


Figure E.1 – General electrical drawing of a CMC

For the measurements described below the CMC line 1 is defined as the CMC winding between pin 1 and pin 2 and line 2 is defined as the winding between pin 3 and pin 4.

E.2.2 S-parameter measurement mixed mode

The test setup for measuring the mixed mode S-parameters consists of a 4-port VNA in combination with a special test board (adapter test board). The test board is included into the test setup during VNA calibration. The reference points for calibration are defined to the pads of the CMC at the test board.



Key

1	Vector network analyzer	3	Reference points for calibration
2	Test board		

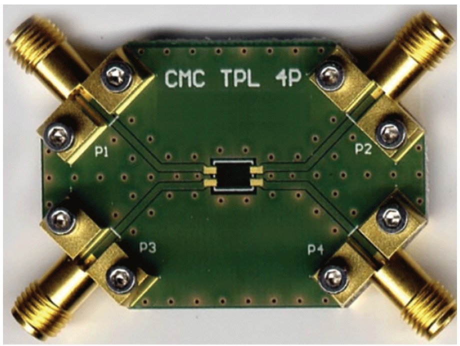
Figure E.2 – Test setup for S-parameter measurements at CMC

The test equipment definitions are the following:

- 4-port vector network analyzer;
- test board S-parameter mixed mode (4-port);
- test board S-parameter single ended (3-port).

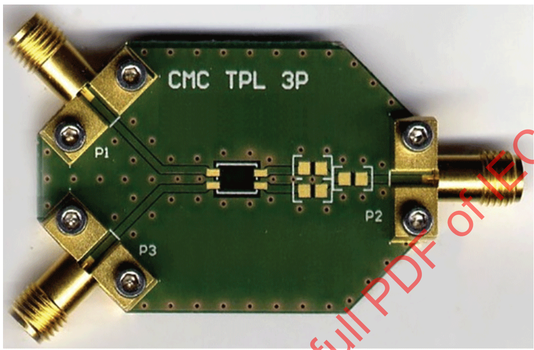
For the S-parameter 3-port test board, additional specific requirements are defined. The 3-port test board with soldered RF connectors used for balance measurement should have a very high grade of self-balance. To ensure the test board self-balance characteristic of symmetrical network at logical port 2 (common mode), the traces between the DUT and all resistors (R1, R2 and R3) must be kept highly symmetric and as short as possible. To verify the test board self-balance characteristic, the test parameter and requirements given in Table E.1 are defined.

Examples for test boards are given in Figure E.3 and Figure E.4.



IEC

Figure E.3 – Example of test board 4-port S-parameter measurement at CMC – mixed mode, top layer

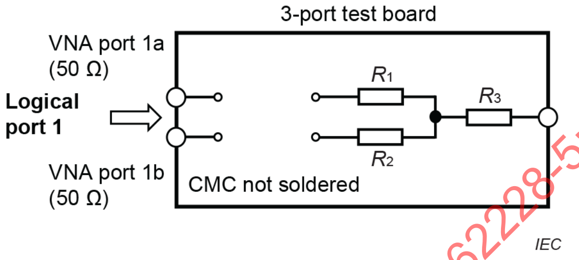


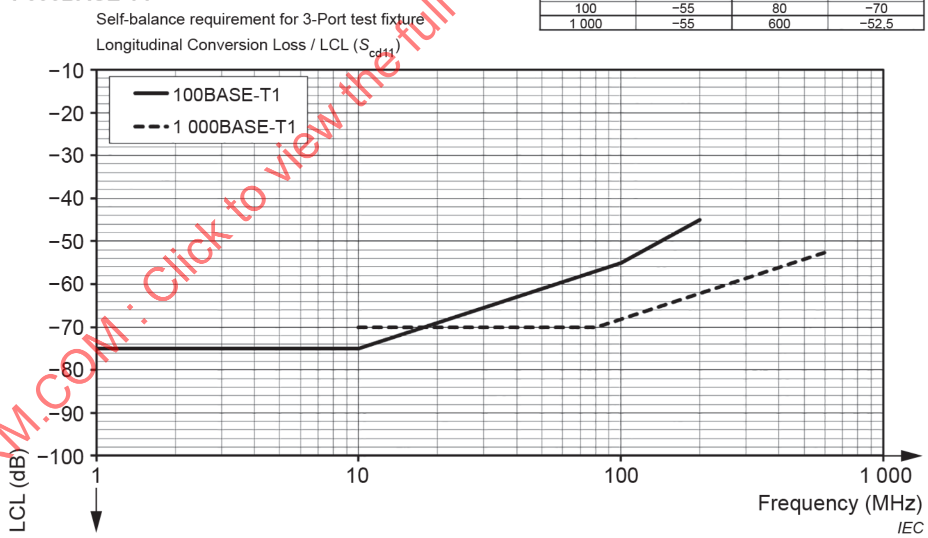
IEC

Figure E.4 – Example of test board 3-port S-parameter measurement at CMC – single ended, top layer

The reference points for calibration are the pads of the CMC footprint at the test board.

Table E.1 – Test procedure and parameters for 3-port test board characterization for CMC

<table>
<tr><th>Parameter</th><th>Description</th></tr>
<tr><td>Frequency range:</td><td>0,3 MHz to 1 GHz</td></tr>
<tr><td>S-parameter:</td><td>S_{dc11} (LCL), logarithmic magnitude in dB / differential port side of 3-port test board.</td></tr>
<tr><td>VNA measurement circuit:</td><td>port definitions:
mixed mode logic port 1: physical port 1a and port 1b
differential mode input (logical port 1): 50 Ω impedance each


R = 49,9 Ω for R_1 and R_2
R = 124 Ω for R_3
The CMC should not be populated at the test board for self-balance measurement.</td></tr>
<tr><td>Requirement for 3-port CMC fixture:</td><td>S – Parameter/CMC for Ethernet 100BASE-T1/ 1 000BASE-T1
<table>
<tr><th>[MHz]</th><th>100BASE-T1</th><th>[MHz]</th><th>1 000BASE-T1</th></tr>
<tr><td>1</td><td>−75</td><td></td><td></td></tr>
<tr><td>10</td><td>−75</td><td>10</td><td>−70</td></tr>
<tr><td>100</td><td>−55</td><td>80</td><td>−70</td></tr>
<tr><td>1 000</td><td>−55</td><td>600</td><td>−52,5</td></tr>
</table>

</td></tr>
</table>

The test procedure and parameters are defined in Table E.2.

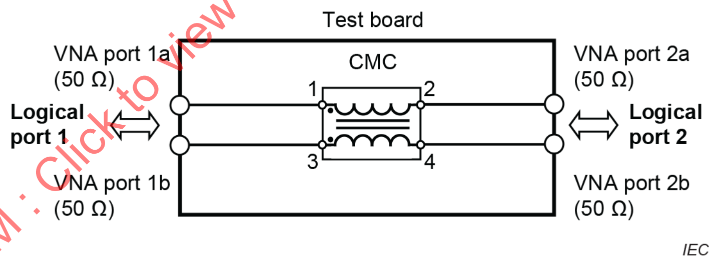
Table E.2 – Test procedure and parameters for S-parameter measurements at CMC

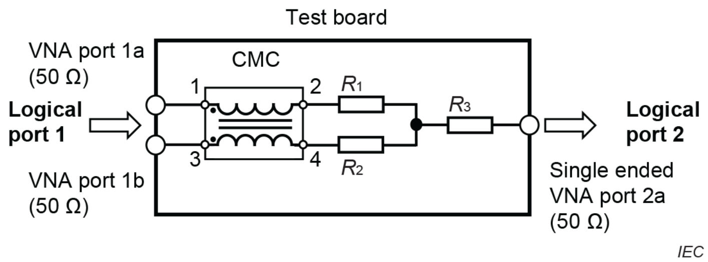
<table>
<tr><th>Item</th><th>Parameter</th></tr>
<tr><td>Frequency range:</td><td>0,3 MHz to 1 GHz</td></tr>
<tr><td>S-parameter per single path:</td><td>4-port parameters
S_{dd11} (RL), logarithmic magnitude in dB / CMC orientation 1
S_{dd22} (RL), logarithmic magnitude in dB / CMC orientation 2
S_{dd21} (IL), logarithmic magnitude in dB
S_{cc21} (CMR), logarithmic in dB

3-port parameters
S_{dc11} (LCL), logarithmic magnitude in dB / CMC orientation 1
S_{dc22} (LCL), logarithmic magnitude in dB / CMC orientation 2
S_{sd21} (DCMR), logarithmic magnitude in dB / CMC orientation 1
S_{sd12} (DCMR), logarithmic magnitude in dB / CMC orientation 2
S_{ds21} (CDMR), logarithmic magnitude in dB / CMC orientation 1
S_{ds12} (CDMR), logarithmic magnitude in dB / CMC orientation 2

For S_{dc22}, S_{sd12} and S_{ds12} measurement the terminal orientation of the CMC is rotated by 180° on the test board.</td></tr>
<tr><td>VNA measurement circuit:</td><td>port definitions:
mixed mode logic port 1: physical port 1a and port 1b
mixed mode logic port 2: physical port 2a and port 2b

pin 1 of CMC is placed on logic port 1.

4-port measurements / S_{dd11}, S_{dd22}, S_{dd21} and S_{cc21} mixed mode:
50 Ω input impedance at each measurement port


3-port measurements / S_{dc11}, S_{dc22}, S_{sd21}, S_{ds21}, S_{ds12} and S_{ds12} single ended:
differential mode input (logical port 1): 50 Ω impedance each
common mode output (logical port 2): single ended network with 200 Ω impedance
$R = (R_1 \parallel R_2) + R_3 + R_{\text{VNA port 2a}}$


R = 49,9 Ω for R_1 and R_2
R = 124 Ω for R_3

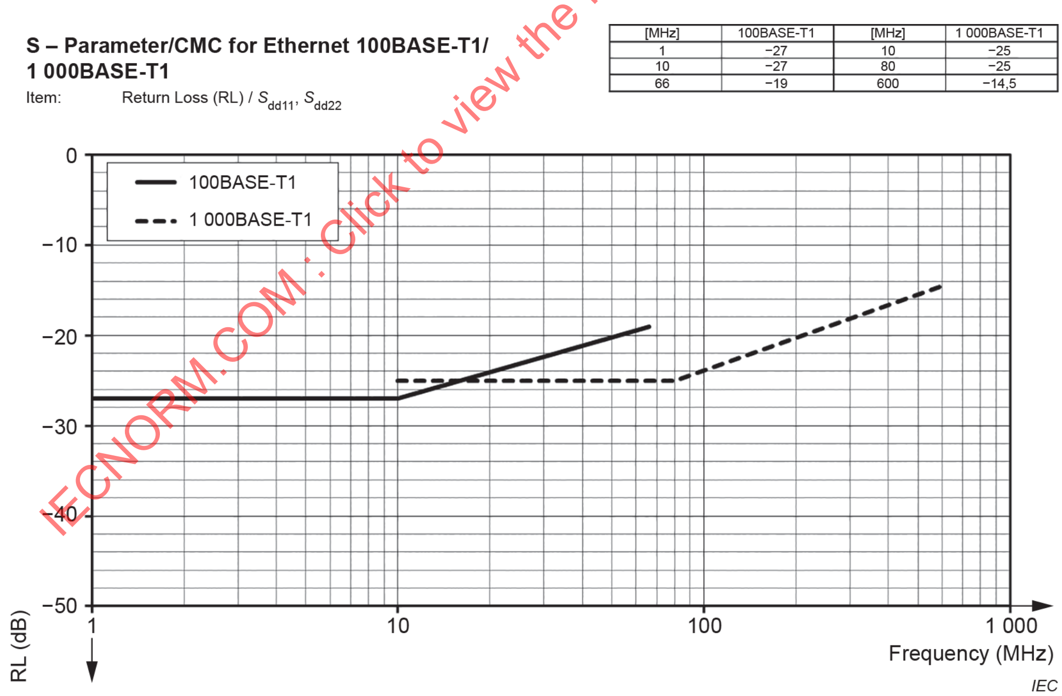
The accuracy of resistor values should be ≤ 1 %. The difference between matching resistors should be ≤ 0,1 %.</td></tr>
</table>

The measurements should be performed and documented according to the scheme given in Table E.3.

Table E.3 – Required S-parameter measurements for CMC

Test	S-parameter	Sample
S1	S_{dd11} (RL)	10 samples each
S2	S_{dd22} (RL)	
S3	S_{dd21} (IL)	
S4	S_{cc21} (CMR)	
S5	S_{dc11} (LCL)	
S6	S_{dc22} (LCL)	
S7	S_{sd21} (DCMR)	
S8	S_{sd12} (DCMR)	
S9	S_{ds21} (CDMR)	
S10	S_{ds12} (CDMR)	

For each test case, the results for all 10 samples should be documented as diagram in the CMC characterization report. Recommended limits for evaluation are given in Figure E.5 to Figure E.9.



[MHz]	100BASE-T1	[MHz]	1 000BASE-T1
1	−27	10	−25
10	−27	80	−25
66	−19	600	−14,5

Figure E.5 – Recommended characteristics for S_{dd11}, S_{dd22} (RL) for CMC

S – Parameter/CMC for Ethernet 100BASE-T1/ 1 000BASE-T1

Item: Insertion Loss (IL) / S_{dd21}

[MHz]	100BASE-T1	[MHz]	1 000BASE-T1
1	−0,5	10	−0,5
10	−0,5	20	−0,5
33	−0,5	100	−0,5
66	−1	400	−1,5

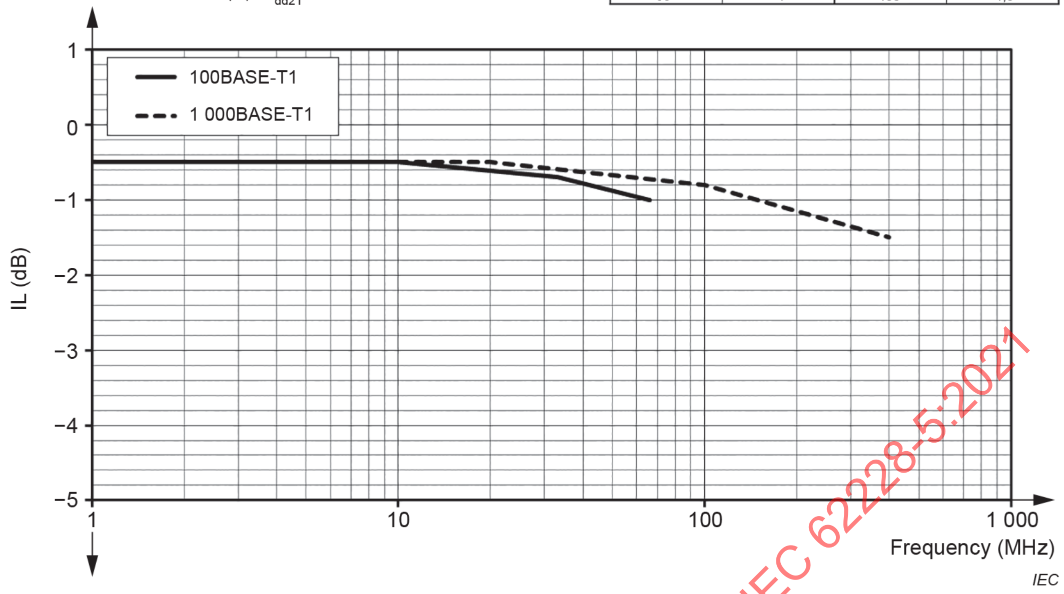


Figure E.6 – Recommended characteristics for S_{dd21} (IL) for CMC

S – Parameter/CMC for Ethernet 100BASE-T1/ 1 000BASE-T1

Item: Common Mode Rejection (CMR) / S_{cc21}

[MHz]	100BASE-T1	[MHz]	1 000BASE-T1
1	−25		
10	−45	10	−32,5
80	−45	30	−42
100	−43	200	−42
200	−37	600	−32,5

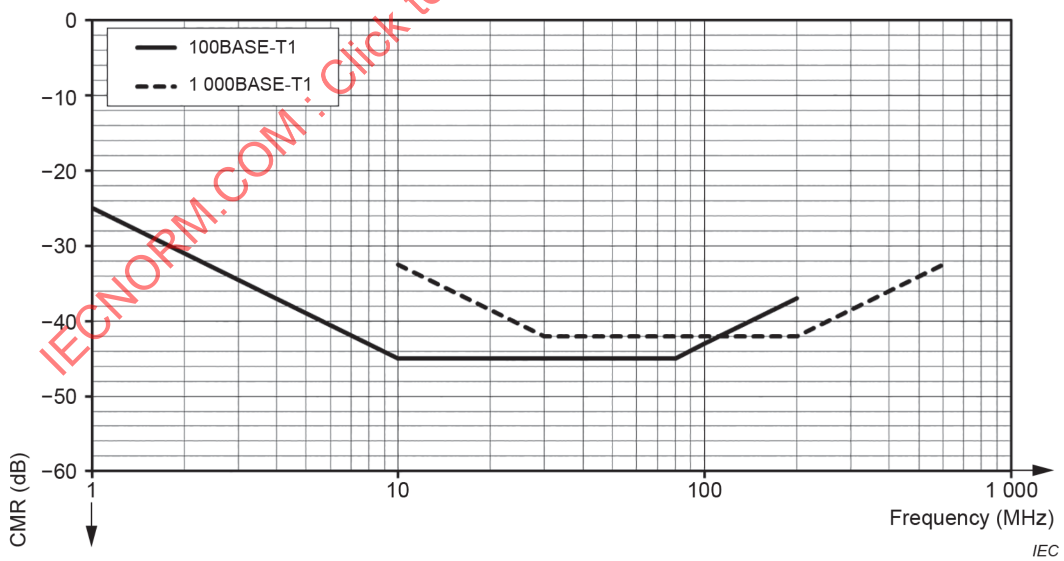


Figure E.7 – Recommended characteristics for S_{cc21} (CMR) for CMC

S – Parameter/CMC for Ethernet 100BASE-T1/ 1 000BASE-T1

Item: Longitudinal Conversion Loss (LCL) / (S_{dd11}, S_{dd22})

[MHz]	100BASE-T1	[MHz]	1 000BASE-T1
1	−50	10	−55
33	−50	80	−55
200	−34,3	600	−45

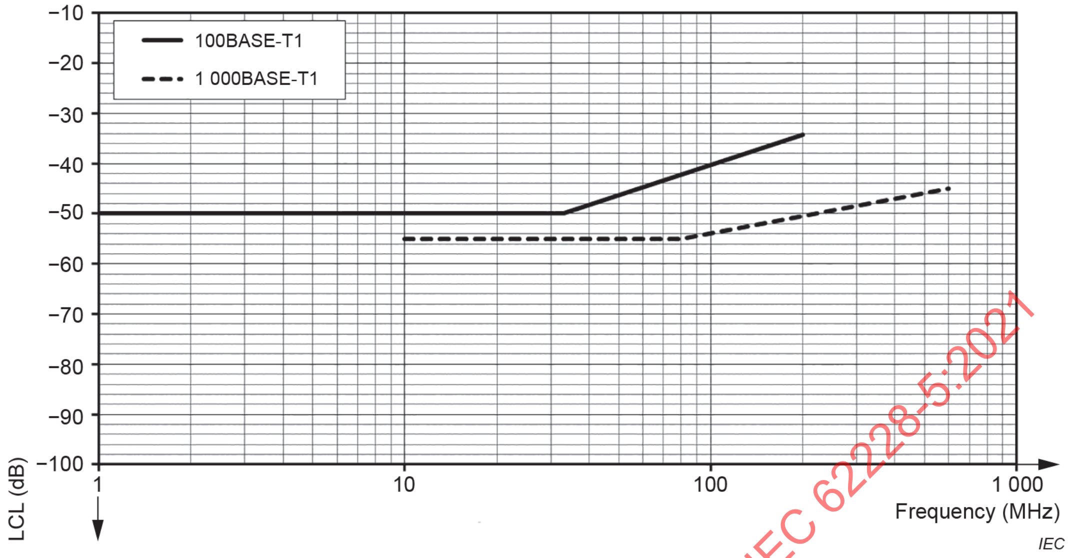
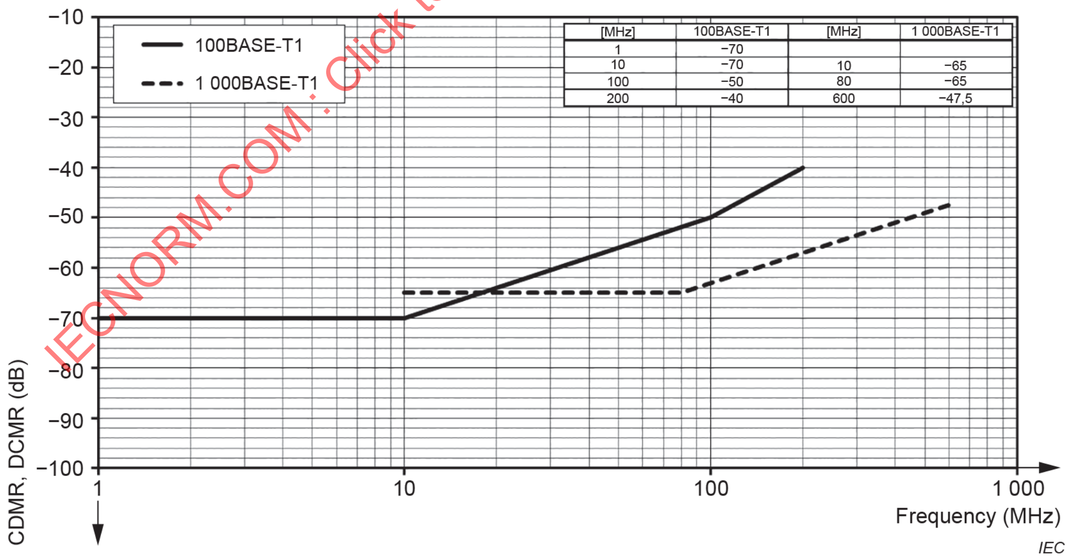


Figure E.8 – Recommended characteristics for S_{dc11}, S_{dc22} (LCL) for CMC

S – Parameter/CMC for Ethernet 100BASE-T1/ 1 000BASE-T1

Item: Common to Differential Mode conversion Ratio (CDMR) / S_{ds21}, S_{ds12}
Differential to Common Mode conversion Ratio (DCMR) / S_{ds21}, S_{ds12}

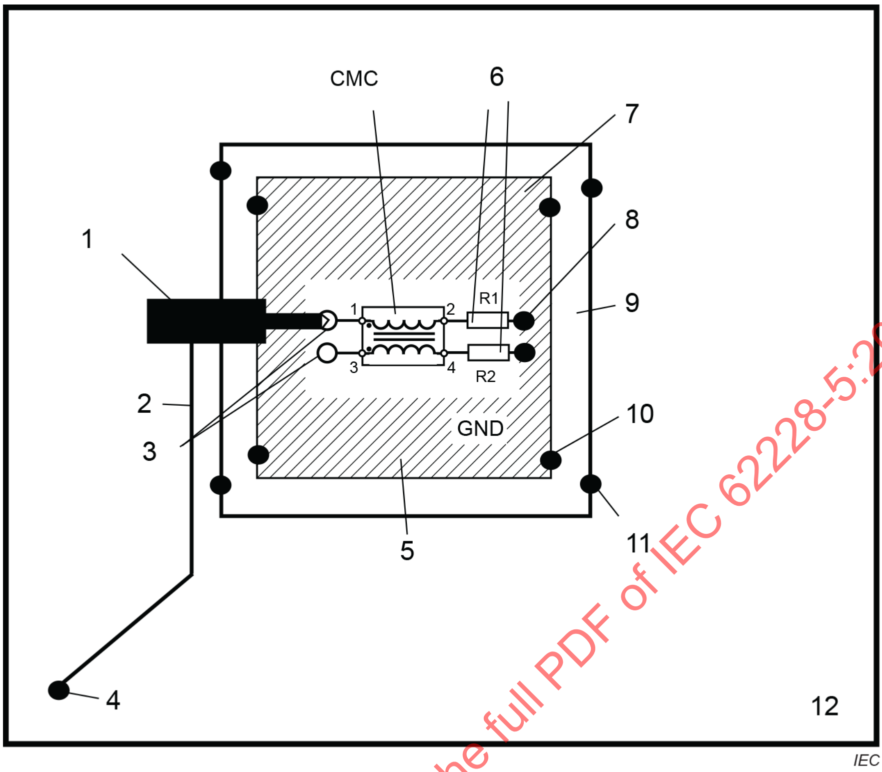


[MHz]	100BASE-T1	[MHz]	1 000BASE-T1
1	−70		
10	−70	10	−65
100	−50	80	−65
200	−40	600	−47,5

Figure E.9 – Recommended characteristics for S_{sd21}, S_{sd12} (DCMR) and S_{ds21}, S_{ds12} (CDMR) for CMC

E.2.3 ESD damage

The test setup given in Figure E.10 is used for testing the ESD robustness of CMC.



Key

1	ESD generator with contact discharge module	7	Ground plane ESD test board
2	ESD generator ground return cable	8	Connection load resistor to ground plane ESD test board
3	Discharge points	9	Metallic test fixture
4	Connection point ground plane	10	Surface connection ESD test board to test board fixture
5	ESD test board	11	Surface connection test board fixture to ground plane
6	Load resistor	12	Ground plane (minimal 0,5 m × 0,5 m)

Figure E.10 – Test setup for ESD damage tests at CMC

The ground plane with a minimum size of 0,5 m × 0,5 m is connected to protective earth of the electrical grounding system of the test laboratory. The ESD generator ground return cable is directly connected to this ground plane.

The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The ground connection of the test fixture is connected to ground plane with low impedance and low inductance. This surface connection should have a contact area of at least 4 cm^2. Copper tapes can be used in addition.

The tip of the ESD generator is directly contacted with one of the discharge points DP1 and DP2 of the ESD test board for testing. For this purpose, the discharge points are implemented as rounded vias in the layout of the ESD test board and are directly connected by a trace 15 (±5) mm with the respective pin of the CMC.

The test equipment definitions are the following:

- ESD generator (according to ISO 10605, discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω);
- ESD test board;
- ground plane;
- test board fixture.

An example for ESD test board is given in Figure E.11.

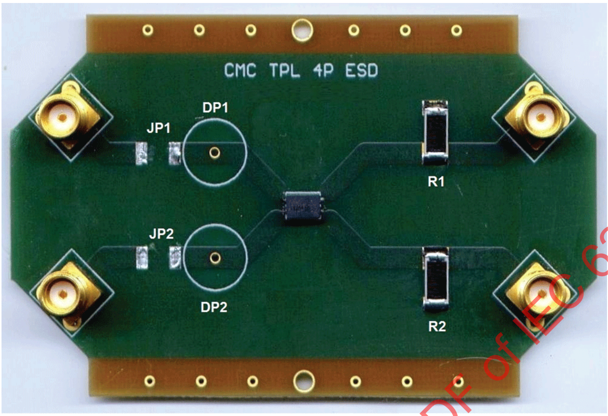


Figure E.11 – Example of ESD test board for CMC, top layer

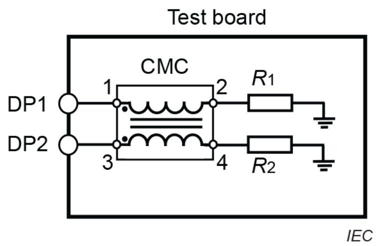
For check of damage evaluation criteria (S-parameter), the reference points for calibration are the input of RF connector (SMA) at the test board.

To achieve a high grade of accuracy of required S-parameter measurements for damage evaluation, it is recommended to use the same test board for S-parameter and ESD tests without re-soldering the DUT.

NOTE For ESD tests, the serial jumpers JP1 and JP2 are left open and the resistors R1 and R2 are populated. For S-parameter measurement the jumpers JP1 and JP2 are closed and the resistors R1 and R2 are not populated.

The required tests and procedure are defined in Table E.4 and should be done on one sample.

Table E.4 – Test parameters for ESD damage tests at CMC

Item	Parameter
Coupling of ESD:	Direct discharge method according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω)
Test circuit:	 R = 2 Ω for R_1 and R_2 All resistors have SMD design 1206 or larger with a maximum tolerance of 2 %. The exact type and manufacturer of the used resistors should be documented in the test report.
ESD test voltage:	± 8 kV

Item	Parameter
Number of discharges:	10 per polarity
Time between discharges:	5 s
Damage evaluation criteria:	– degrade by more than 0,1 dB from the initial value after performing the tests for S-parameter S_{dd21} for frequencies $f \leq 200$ MHz – degrade by more than 1 dB from the initial value after performing the tests for S-parameter S_{dd11}, S_{dd22} and S_{cd21} for frequencies $f \leq 200$ MHz The S-parameter measurements should be done according to E.2.2. Frequency ranges or frequency spots with a level at noise floor or below the related limits of E.2.2 should not be weighted for applying the damage evaluation criteria. For simplification of measurement for check of mode conversion loss the S-parameter S_{cd21} is used instead of S_{sd21}. The setup for S-parameter S_{cd21} is same as used for the other required S-parameter. Because of different test circuitry for S-parameter S_{cd21} and S_{sd21} the related limit for S-parameter S_{cd21} is corrected by +10 dB.
Test procedure:	1 S-parameter reference measurement before ESD test 2 apply ESD discharges at DP1 (± 8 kV, 10 per polarity, 5 s delay) 3 apply ESD discharges at DP2 (± 8 kV, 10 per polarity, 5 s delay) 4 demagnetization of CMC (if needed) 5 evaluate damage using damage evaluation criteria If a damage occurs at ± 8 kV the test should be repeated with a reduced ESD test voltage to find out the immunity threshold of the DUT. Nevertheless, applying an ESD test voltage of ± 8 kV without damage for DUT is required to pass the test.

The measurements should be performed and documented according to the scheme given in Table E.5.

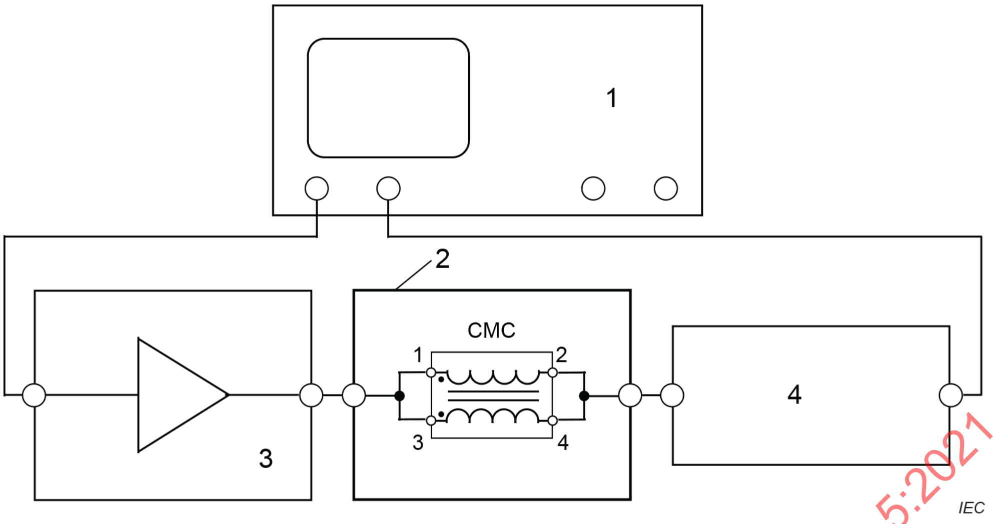
Table E.5 – Required ESD tests for damage for CMC

Test	Discharge point	Comment	Sample
E1	DP1	Line 1	1 sample
E2	DP2	Line 2	

The CMC should withstand the ESD discharge without damage according to the damage evaluation criteria up to ± 8 kV.

E.2.4 Saturation test at RF disturbances

The test setup for measuring the saturation effect at RF immunity tests consists of a 4-port VNA or 2-port VNA in combination with a RF amplifier, RF attenuator and a special test board. The test setup is given in Figure E.12.



Key

1	Vector network analyzer	3	RF amplifier 50 Ω, typically 40 dB
2	Test board	4	RF attenuator 50 Ω, 40 dB

Figure E.12 – Test setup for RF saturation measurements at CMC

The test equipment definitions are the following:

- 4-port or 2-port vector network analyzer;
- RF amplifier (impedance 50 Ω, gain app. 40 dB, $P_{CW} \geq 10$ W);
- RF attenuator (impedance 50 Ω, attenuation 40 dB), and
- test board RF saturation / S-parameter (2-port).

An example for RF saturation / S-parameter test board is given in Figure E.13.

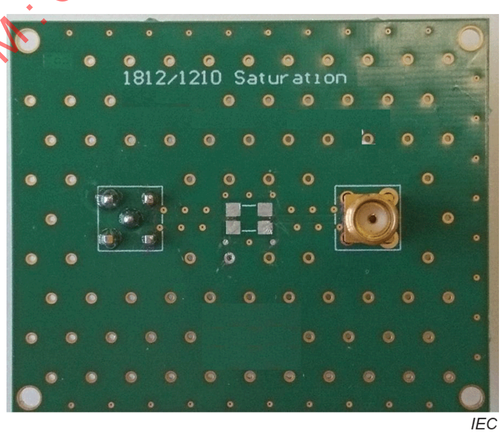
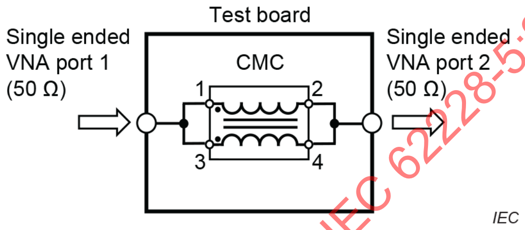


Figure E.13 – Example of RF saturation / S-parameter test board for CMC, top layer

The required test procedure and parameters are defined in Table E.6. The test should be done on one sample.

Table E.6 – Test procedure and parameters for RF saturation tests at CMC

Item	Parameter
Frequency range:	1 MHz to 1 GHz
S-parameter power level:	S_{21} (CMR), logarithmic magnitude in dB
Measurement test circuit:	port definitions: logic port 1: physical port 1 logic port 2: physical port 2 line 1 of CMC is placed on transceiver side (logic port 1) S_{21} measurement: 50 Ω input impedance at each measurement port 
Test power level:	forward power: 24 dBm, 30 dBm, 33 dBm, 36 dBm These test levels are obtained from test level measurement into a 50 Ohm load.
Dwell time per power level:	≥ 60 s
Evaluation of saturation effect:	maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 30 dBm maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 33 dBm above 5 MHz maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 36 dBm above 7 MHz
Test procedure:	1 define the test equipment settings for test power levels 24 dBm, 30 dBm, 33 dBm and 36 dBm with replacement of DUT by short connections on the test board 2 test with power level 24 dBm for setting the reference value 3 test with power level 30 dBm and evaluation 4 test with power level 33 dBm and evaluation 5 test with power level 36 dBm and evaluation

The tests should be performed and documented according to the scheme given in Table E.7.

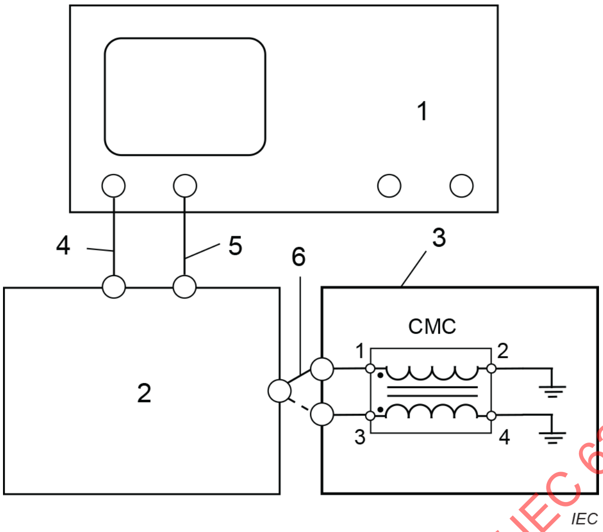
Table E.7 – Required RF saturation tests for CMC

Test	S-parameter	Sample
RFS1	S_{21} (CMR)	1 sample

The CMC should withstand the RF power saturation test according to the evaluation criteria up to a power amplitude of 36 dBm.

E.2.5 Saturation test at ESD

The test setup for measuring the saturation effect at ESD tests consists of a TLP test system, digital storage oscilloscope and a special test board. The test setup is given in Figure E.14.



Key

1	DSO	4	TLP current
2	TLP test system	5	TLP voltage
3	Test board	6	TLP pulse

Figure E.14 – Test setup for ESD saturation measurements at CMC

The test equipment definitions are the following:

- TLP test system according to IEC 62615, including TLP generator, current probe and voltage probe;
- digital storage oscilloscope (DSO, 50 Ω input impedance, minimum 4GHz analog input bandwidth);
- test board CMC ESD saturation.

An example for CMC ESD saturation test board is given in Figure E.15.

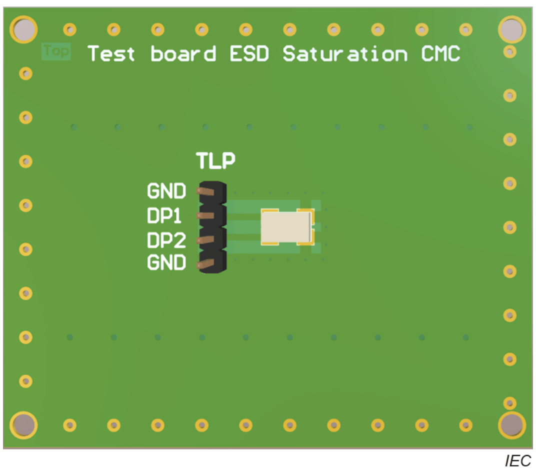
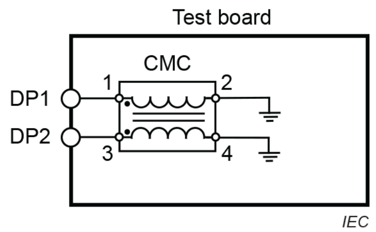


Figure E.15 – Example of ESD saturation test board for CMC, top layer

The required test procedure and parameters are defined in Table E.8. The test should be done on one sample.

Table E.8 – Test procedure and parameters for ESD saturation tests at CMC

Item	Parameter
Coupling of ESD:	TLP test system according to IEC 62615
Test circuit:	
TLP test parameter:	Current pulse width: 100 ns Current rise time: ≤ 1 ns Measurement time window: 70 ns to 90 ns Maximum test voltage: 500 V Test voltage step size: ≤ 2 V Maximum test current: 15 A
Evaluation of saturation effect:	CMC ESD saturation break down voltage V_{ESD_br} derived from measured TLP I/V characteristic and limits according to Table E.10.

The tests should be performed and documented according to the scheme given in Table E.9.

Table E.9 – Required ESD saturation tests for CMC

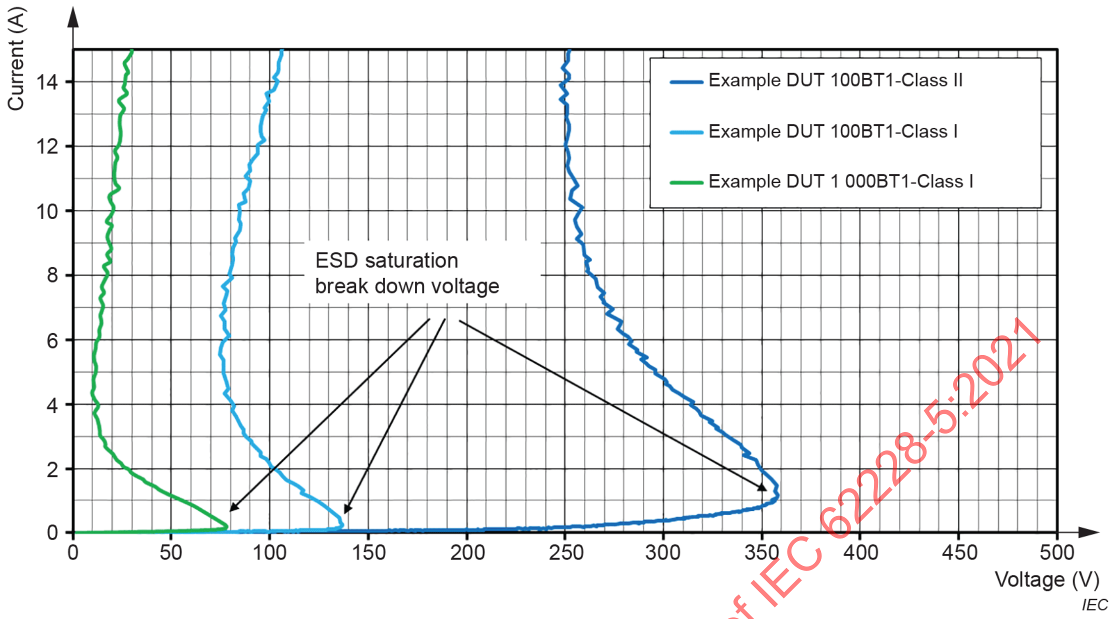
Test	Discharge point	Comment	Parameter	Sample
ES1	DP1	Line 1	CMC ESD saturation break down voltage	1 sample
ES2	DP2	Line 2		

For each test case, the TLP I/V characteristic should be recorded and documented in a diagram in the test report. The derived CMC ESD saturation break down voltage should be classified according to the recommended limits given in Table E.10.

Table E.10 – ESD saturation break down voltage classes for CMC

Ethernet system	Class	V_{ESD_br}
100BASE-T1	I	125 V to 325 V
	II	≥ 325 V
1000BASE-T1	I	50 V to 125 V
	II	≥ 125 V

An example of measurement results for typical CMCs is shown in Figure E.16.

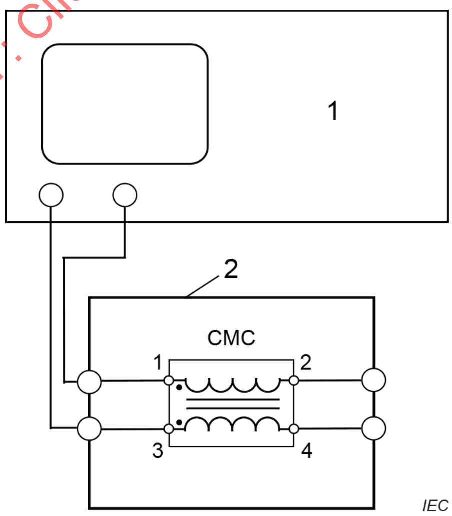


ESD saturation break down voltage	Limit Class II	Limit Class I
100BASE-T1	>325 V	125 V to 325 V
1 000BASE-T1	>125 V	50 V to 125 V

Figure E.16 – Example of ESD saturation tests results for CMC

E.2.6 TDR measurement of differential mode impedance

This test is only for information purpose and can be used for additional interpretation of results of S-parameter measurements. The test setup for measuring the differential mode impedance consists of a two-channel TDR test equipment and a special test board. The test setup is given in Figure E.17.



Key

1 TDR test equipment
2 Test board

Figure E.17 – Test setup for TDR measurement at CMC